|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Roll No |  |  |  |  |  |  |  |  |  |  |  |  |

 ****

**Presidency University**

**Bengaluru**

 **SCHOOL OF ENGINEERING**

 **MAKE UP EXAMINATION – JULY 2024  SET-A**

**Date**: 04/July/2024

**Time**: 1:30pm – 4:30pm

**Max Marks**: 100

**Weightage**: 50%

**Semester**: II & III

**Course Code**: ECE2007

**Course Name**: Digital Design

**Department:** Computer Science and Engineering

 **Instructions:**

1. *Read the all questions carefully and answer accordingly.*
2. *Do not write any matter on the question paper other than roll number.*

**PART A**

**Answer any SIX Questions. Each question carries 10 marks. (6Qx 10M= 60M)**

1. A flip flop is a sequential circuit which consist of single binary state of information or data. The digital circuit is a flip flop which has two outputs and are of opposite states. Briefly discuss working of NAND based JKFF along with the truth table, Characteristic table , Excitation table and obtain equation for the tables. (CO:3 BL: Comprehension)
2. A comparator is a device that compares two bits, voltage or currents and outputs a digital signal indicating which is larger. Design a 2-Bit comparator with the help of truth table and obtain the logical expression for each case with the help of simplification method (K-map).

(CO:2 BL: Comprehension)

1. Boolean Minimization is important since it reduces the cost and complexity of the associated circuit.
a. Convert the given below expression to simplified SOP (Sum of Product) form of the Boolean expression (P + Q' + R'). (P + Q' + R). (P + Q + R')

b. Convert the given expression: F(P, Q, R) = PQ + QR' + PR' into Canonical  SOP form.

(CO:1 BL: Comprehension)

1. The multiplexer is a combinational logic circuit designed to switch one of several input lines to a single common output line by the application of a control logic. The input has a maximum of 2^N data inputs (where N = selection or control lines) and single output line.

Implement F( A,B,C,D)=∑m(0,3,5,7,9,12,13) + d(2,6,8)
i) Implement using 8:1 MUX.
ii) Implement using logic gates.

(CO:2 BL: Comprehension)

1. Roy and family are interested to design a block that has 16 input lines and 1-bit output and that block is named as Multiplexer that performs reverse operation of a De -Multiplexer. Help them to build the block but they have only 2:1 MUX Hence, implement 16:1 MUX using 2:1 MUX.

(CO:2 BL: Comprehension)

1. A decoder is a device that generates the original signal as output from the coded input signal and converts n lines of input into 2^n lines of output. Interpret full adder using 3 to 8 decoder (CO:2 BL: Comprehension)
2. A digital system is to be designed in which the month of the year is given as input in binary form. The month January is represented as '000', February '001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0'. Design and implement the logic for only 8 months from (January to August). Consider the system of three variables (A, B, C). Design and implement the simplified logic using NAND gates only.

(CO:1 BL: Comprehension)

1. Any number can be represented in various base systems. From the truth table below, determine the standard SOP expression



(CO:1 BL: Comprehension)

**PART B**

**Answer any TWO Questions. Each question carries 20 marks. (2Qx 20M= 40M)**

1. Before take-off, the pilot of an aircraft carry out preflight safety checks for the switches. When all checks have been completed, they will show a green signal to run the engine. The Engine failure will take place if the following conditions arise:
* Switch B is OFF and switches C, D are ON at same time.
* Switches C and D are OFF but switch B is ON at same time.
* Switches B and C are ON but switch D is OFF at same time.

Assume that the switches provide logic level 0 in OFF position and logic level 1 in their ON position and engine failure as logic 0.

1. Derive the truth table for this system
2. Design, using Karnaugh Map techniques, a minimum AND-OR gate network for this system. Draw the resulting digital circuit diagram.

 (CO:1 BL: Application)

1. The below given circuits is a small part of a huge logic circuit. To implement this logic, minterms or canonical form is needed. Using the circuit estimate X

(a)



 (b)

(CO:1 BL: Application)

1. In digital logic circuits, a counter is a sequential logic circuit which stores the number of times a particular event or process has occurred, often in relationship to a clock. Design a synchronous 3 bit UP counter using JK flip flop with its state diagram, state table, and excitation table along with flip flop input equations.

 (CO:3 BL: Application)