|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Roll No |  |  |  |  |  |  |  |  |  |  |  |

PRESIDENCY UNIVERSITY BENGALURU

 SCHOOL OF INFORMATION SCIENCE

 MAKEUP EXAMINATION – JULY 2024

|  |  |
| --- | --- |
| **Semester : 6th Sem** | **Date : 2nd July 2024** |
| **Course Code : ECE3014** | **Time : 1:30pm – 4:30pm** |
| **Course Name : Microcontroller Applications** | **Max Marks : 100** |
| **Program : B.Tech** | **Weightage : 50%** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

|  |
| --- |
| **PART A** |
|  **ANSWER ANY 5 QUESTIONS 5Q X 2M=10M** |
| 1 | The amount of RAM and ROM on chip is one of the criteria for choosing a microcontroller. What is the difference between byte addressable memory and bit addressable memory?  | (CO 1) | [Knowledge] |
|  |
| 2 | There are four major 8-bit microcontrollers and each of these microcontrollers has a unique instruction set and register set. What is the function of PC register in 8051 microcontroller?  | (CO1) | [Knowledge] |
|  |
| 3 | Machine cycle refers to a sequence of steps that a computer's central processing unit (CPU) goes through in order to execute a single machine language instruction. Name the instruction used to waste the clock cycles and how many machine cycles are taken for the execution for the same.  | CO2 | [Knowledge] |
|  |
| 4 | Consider the below set of instructions which are interrelated as single program. Write the status of registers after execution of every instruction. Assume that initially, the contents of the registers A and B are 66H and 77H respectively.  | (CO2) | [Knowledge] |
|  |
| 5 | Data communication can be done in three modes. Distinguish between half duplex and full duplex mode of communications | (CO3) | [Knowledge] |
|  |
| 6 | Seial data transfer in 8051 is done at various baud rates. How can the baud rate of data transfer be doubled | (CO3) | [Knowledge] |
|  |  |  |  |
| 7 | Banked registers in ARM are available only when the processor is in particular mode. Name the banked registers used in Abort mode.  | (CO4) | [Knowledge] |
|  |

|  |
| --- |
| **PART B** |
|  **ANSWER ANY 5 QUESTIONS 5Q X 10M=50M** |
| 8 | a) Assembler directives in 8051 assembly language are instructions that guide the assembler during the process of assembling. Discuss different assembler directives in 8051 microcontroller.     (CO1)    5Mb) With timing diagram, explain the signals used to access external ROM & RAM in  8051 based system   (CO1)    5M | (CO1) | [Comprehension] |
|  |
| 9 | Assembly language is a low-level language that helps to communicate directly with computer hardware. Attempt the following questions:a) Write an ALP to find number of 1's appearing in the 8 bit data 25H and store it in the RAM location 25H         (5 Marks)b) Write the addressing modes of the instruction given below:        MOV A, R1        SWAP A        ADD A, @R0       SUB A, 2000H       SUB A, #2000H (5 Marks) | (CO2) | [Comprehension] |
|  |
| 10 | Serial communication can be controlled using two dedicated registers.a) Identify the two registers and explain the bit configuration of any one in detail.b) Assuming a crystal frequency of 11.0592MHz Write a program to receive serial data and place it in internal RAM location 65H and also send it to Port 2 | (CO3) | [Comprehension] |
|  |
| 11 | Intel 8051 can be programmed in different modes to generate software delays. Calculate the value to be loaded into the Timer register to generate a delay of 3msec with crystal frequency of 11.0592MHz for (i) Mode 0 and  (ii) Mode 1  and write the programs in both the modes. | (CO3) | [Comprehension] |
|  |
| 12 | An embedded system is a dedicated system designed to perform one or two specific functions. Identify the key component used in the design of embedded system. Explain the 4 major design rules and also its design philosophy with relevant diagram. | (CO4) | [Comprehension] |
|  |
| 13 | The on-chip memory capacity of the 8051 microcontroller can be increased to extend the functionalities of the controllers. Design a microcontroller system to interface 8051 to 8KB RAM and 16KB ROM with a neat diagram and memory map. | (CO1) | [Comprehension] |
|  |  |  |  |
| 14 | A given assembly language program is a series of statements or lines which are either assembly language instructions or statements called directives. Identify valid instruction and also identify the addressing mode and mention the output at each line.(a) MOVC A, @A+DPTR ; A = 06H, DPTR = 01FAH(b) MOV A, @R3 ; R3 = 54H, Data in 54H = 3EH(c) MOV R4, R6 ; R6 = 29H(d) The instruction to tranfer data from R2 of RB0 to R4 of RB2 will be \_\_\_\_\_ | (CO2) | [Comprehension] |
|  |

|  |
| --- |
| **PART C** |
|  **ANSWER ANY 2 QUESTIONS 2Q X 20M=40M** |
| 14 | Suppose you are a design engineer at ARM®. Two pass codes are coming through the system. Each pass code is 8 bits long. The format of the pass code is PQ and RS. Here P, Q, R, and S are nibbles. The numbers PQ and RS are by default available in locations 30H and 40H respectively.  Your job is to give the system a new pass code which is generated by using the following arithmetic operation.http://guqbms.inpods.com:57953/api/v1/downloadFile?fileId=22856&tenantid=13Prepare a program in 8051 Assembly Language to perform the same and store the new passcode in location 50H. | (CO2) | [Application] |
|  |
| 15 | Assume that the 8051 serial port is connected to the COM port of the IBM PC, and on the PC we are using the HyperTerminal program to send and receive data serially. Program the 8051 to send to the message “We Are Ready” to the PC serially continuously using the 4800 baud rate. | (CO3) | [Application] |
|  |
| 16 | a) Serial communication is preferred over parallel communication for the data transfer over long distance. Write a program for the 8051 to transfer “PRESIDENCY” serially at 9600 baud, 8-bit data, 1 stop bit, do this continuously.  (CO3)  10Mb) Processors with RISC architecture are faster as compared to their counterparts with CISC architecture. What mechanism does RISC processor use to do faster execution of instructions? Explain the same with relevant diagram            (CO4)  10M     | (CO3) | [Application] |
|  |
|  |