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PRESIDENCY UNIVERSITY BENGALURU

 SCHOOL OF ENGINEERING

 MAKE UP EXAMINATION – JULY 2024

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| **Semester : I**  | **Date : 3 July 2024** |
| **Course Code : ECE2009** | **Time : 09:30 am – 12:30 pm** |
| **Course Name : Digital Computer Fundamentals** | **Max Marks :100** |
| **Program :B. Tech. (ECE)** | **Weightage :50%** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 2 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

**PART A**

**Answer any SIX Questions. Each question carries 10 marks. (6Q x 10M = 60M)**

1. Briefly discuss working of NAND based D FF along with the truth table, Characteristic table, Excitation table and obtain equation for the tables. (CO:3 BL: Comprehension)
2. Design a 2-Bit comparator with the help of truth table and obtain the logical expression for each case with the help of simplification method (K-map). (CO:2 BL: Comprehension)
3. (a) Convert the given below expression to simplified SOP (Sum of Product) form of the Boolean expression

$$F\left(A, B, C\right)=\left(A+\overbar{ B }+\overbar{ C }\right)\left(A+\overbar{ B }+C\right)\left(A+B+\overbar{ C }\right)$$

(b) Convert the given expression: $F\left(A, B, C\right)=A.\overbar{ C }+\overbar{ A }.B+\overbar{ A }.\overbar{ C }$ into Canonical  SOP form.

(CO:1 BL: Comprehension)

1. Implement the following MUX using only 2:1 MUX
	1. 4:1 MUX
	2. 8:1 MUX

(CO:2 BL: Comprehension)

1. Draw the truth table of a 3:8 decoder. Write the expression for the outputs. Now draw the truth table of a full adder. Implement the full adder using a 3:8 decoder.

(CO:2 BL: Comprehension)

1. A digital system is to be designed such that there are 3 inputs A, B, and C, where A, B, C are single bits. The output, Y is 1 only when the decimal equivalent of ABC is divisible by 2. Draw the truth table and find a simplified expression for the output X and hence draw the logic circuit. Note the decimal equivalent 0 is considered as don’t care in the design.

(CO:1 BL: Comprehension)

1. Draw the circuit diagram of a Parallel In Serial Out Shift register and explain the working

(CO:3 BL: Comprehension)

1. Realize the following expressions using NAND gate ONLY
	1. $Y=A.B.\overbar{ C }+A.\overbar{ B }+C.\overbar{ A }$
	2. $Y=\left(B+\overbar{ C }+A\right).(\overbar{ B }+C).\overbar{ A }$

(CO:2 BL: Comprehension)

**PART B**

**Answer any TWO Questions. Each question carries 20 marks. (2Qx 20M= 40M)**

1. Before take-off, the pilot of an aircraft carry out preflight safety checks for the switches. When all checks have been completed, they will show a green signal to run the engine. The Engine failure will take place if the following conditions arise:
* Switch B is OFF and switches C, D are ON at same time.
* Switches C and D are OFF but switch B is ON at same time.
* Switches B and C are ON but switch D is OFF at same time.

Assume that the switches provide logic level 0 in OFF position and logic level 1 in their ON position and engine failure as logic 0.

1. Derive the truth table for this system
2. Design, using Karnaugh Map techniques, a minimum AND-OR gate network for this system. Draw the resulting digital circuit diagram.

(CO:1 BL: Application)

1. In digital logic circuits, a counter is a sequential logic circuit which stores the number of times a particular event or process has occurred, often in relationship to a clock. Design a synchronous 3 bit UP counter using JK flip flop with its state diagram, state table, and excitation table along with flip flop input equations. (CO:3 BL: Application)
2. Draw the truth table of the following function

$$f\left(A, B, C\right)=∑m\left(2, 5, 6, 7\right)$$

Realize the function using

* 1. 8:1 MUX ONLY
	2. One 4:1 MUX and logic gates

(CO:2 BL: Application)