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PRESIDENCY UNIVERSITY BENGALURU

SCHOOL OF ENGINEERING

MAKE-UP EXAMINATION - JULY 2024

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| **Semester : V** | **Date : 15.07.2024** |
| **Course Code :ECE3008** | **Time : 01:30 PM -04:30 PM** |
| **Course Name :VLSI Design** | **Max Marks :100** |
| **Program :B.Tech (ECE)** | **Weightage :50%** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

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| **PART A** | | | |
| **ANSWER ANY 4 QUESTIONS 4Q X 5M=20M** | | | |
| 1 | VLSI circuits are found in a variety of places, including your computer, automobile, digital camera, cell phones, and so on.  List out the advantages and applications of VLSI design. | (CO 1) | [Knowledge] |
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| 2 | A half adder is a basic building block in parallel adder circuit.  Design a half adder circuit and write Verilog HDL code for half adder in gate level modelling. | (CO 1) | [Knowledge] |
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| 3 | The threshold voltage of a MOSFET is the value of the gate voltage when a conductive band forms between the transistor's source and drain.  (i) Determine the value of VT , if γ = 0.2/v2 , εox = 4ε0 , tox = 0.2Å  (ii) Determine the drain current for saturation region is VT= 1.05V, VGS = 4V, k = β/2= 0.4\*10-3 | (CO 2) | [Knowledge] |
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| 4 | The MOSFET is the most common type of transistor today. Their primary use is to control conductivity, or how much electricity can flow, between its source and drain terminals based on the amount of voltage applied to its gate terminal.  Draw the band diagram of the MOSFET during, accumulation, Inversion and depletion. | (CO 2) | [Knowledge] |
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| 5 | Find the critical voltages and noise margins for a CMOS inverter, with the following values: VDD = 5.0 V, VTHn = 0.4 V, VTHp = −0.4 V, Kn = 50 μA/V2 & Kp = 20 μA/V2. | (CO 2,3) | [Knowledge] |
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| 6 | Stick diagrams show the layers used and the relative position of the layer.  Draw the stick diagram for 2 input CMOS NAND gate. | CO 2, 3) | [Knowledge] |
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| **PART B** | | | |
| **ANSWER ANY 5 QUESTIONS 5Q X 10M=50M** | | | |
| 7 | The VLSI design flow is a complex and iterative process that involves collaboration among designers, verification engineers, and physical designers.  Draw the VLSI design flow diagram and describe it. | CO 4) | [Comprehension] |
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| 8 | ASIC is a custom design for particular task and applications. Describe the standard cell and gate array-based ASICs. | (CO 3,4) | [Comprehension] |
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| 9 | Threshold voltage in a MOSFET is defined as the minimum voltage required for the device to start conducting.  (i) Write the Threshold voltage expression and indicate each parameter.  (ii) What will happen if there is non-zero substrate voltage applied? | (CO 4) | [Comprehension] |
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| 10 | MOS transistor switches ON when a proper voltage is applied at the gate terminal. Calculate the current flow in the NMOS with the following parameters. L= 2µm. W =10 µm, µn = 0.05m2/v.s, Cox = 1.5\*10--4 F/m2, VT0 = 0.4V.  i). VGS = 0.45v, VDS = 0 V  ii). VGS = 0.3 v, VDS = 0 V  iii). VGS = 0.8 v, VDS = 0.4 V  Identify the region of operation. | (CO 3,4) | [Comprehension] |
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| 11 | The reduction of all dimensions of the chip by a factor of “s” is called scaling. Scale the below parameters using the three scaling techniques.  i. Gate capacitance per unit area ii. Charge density in the channel  iii. Channel resistance | (CO 4) | [Comprehension] |
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| 12 | MOS transistors suffer from unwanted parasitic effects. One such problem in MOSFET is latch up.  With a neat figure explain latch up and mention its prevention techniques. | (CO 3,4) | [Comprehension] |
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| 13 | The DC analysis of the inverter is a function of the output voltage (Vout) with respect to the input voltage (Vin). Describe DC analysis of CMOS inverter. | (CO 4) | [Comprehension] |
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| **PART C** | | | |
| **ANSWER ANY 2 QUESTIONS 2Q X 15M=30M** | | | |
| 14 | Mutiplxer is also known as data selector. Design 4:1 mux and write Verilog HDL code in all three modelling. | (CO 5) | [Application] |
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| 15 | The fabrication process in VLSI technology involves several steps that are crucial in producing a functional integrated circuit.  Write short note on CMOS N-well Process | (CO 5) | [Application] |
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| 16 | (i) The parallel connection of PMOS and NMOS known as Transmission Gate (TG) and TG is used to implement digital logic circuits. Design 2:1 mux using TG and list out the advantages of transmission gate. (8)  (ii) Two inverters are back-to-back connected to form the Static Random Access Memory (SRAM) cell. Draw the SRAM-6T memory cell. (7) | (CO 5) | [Application] |
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