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**Presidency University**

**Bengaluru**

**SCHOOL OF ENGINERING**

**Make-Up Examinations, July 2024**

**Semester**: 7

**Course Code**: ECE 3048

**Course Name**: Fpga for embedded system

**Program** : B Tech

**Date**: 10/7/2024

**Time**: 01:30 PM– 4:30 PM

**Max Marks**:100

**Weightage**: 50 %

**Instructions:**

1. *Read the all questions carefully and answer accordingly.*
2. *Do not write any matter on the question paper other than roll number.*

**Part A [Memory Recall Questions]**

**Answer all the Questions. Each question carries Two marks. (5Qx 4M= 20M)**

1. If we need a little logic to implement, we will choose CPLD and for a complex function we will use FPGA. There are many markets player to provide the solution for the same. Mention four popular vendors who provide FPGA.?

(C.O.No.1) [Knowledge Level]

1. The first programable logic device was developed in 1956 and commercially made available in 1971. Name this logic device and draw its structure in detail?

(C.O.No.1) [Knowledge Level]

1. Configurable logic block makes FPGA more suitable choice for the designer. Explain various components of these programable blocks.

(C.O.No.2) [Knowledge Level]

1. In competitive environment, chip development cycles are compressed, causing design teams to reuse semiconductor Intellectual Property (IP) to accelerate time to market. List the types of Ip core available and classify them correctly?

(C.O.No.3) [Knowledge Level]

1. Data types in Verilog inform the compiler whether to act as a transmission line (like a wire) or store data. Describe the data types NET and REG with example ?

(C.O.No.2) [Knowledge Level]

**Part B [Thought Provoking Questions]**

**Answer all the Questions. Each question carries Ten marks. (5Qx10M=50M)**

1. PLA and PAL are part of SPLD and also contribute to the development of CPLD family devices in earlier generations. Implement the given Boolean equation using PAL and PLA. As per implementation suggest your comment on each design.  
   F=AB’+AC’B+B’C’ (C.O.No1 )[Comprehensive Level ]
2. Hardware description language plays a role in deciding the target FPGA device for design.   
   (a) List various styles of modeling as per Y chart of the modeling [4]   
   (b) If you have been asked to design combinational logic shown below using Verilog, Which method you will select and also write Verilog code using that method [1+5]

(C.O.No.1) [Comprehensive Level ]

1. Embedded systems are programmed using embedded programming. Define embedded systems. With the help of system level architecture describe the embedded systems. List the various operating systems available for specific applications such as agriculture and medical application.
2. The FPGA dominates the programable logic world and most importantly, it also helps to develop fast solutions for the Embedded designs.  
   (a) Discuss various types of types FPGAs [6]  
   (b) List out all the components of FPGA
3. Once we create soft core processor, most important part is programming a soft-core processor.   
   (a) Mention various software platforms available to programme softcore processor.  [2]  
   (b) Name software interface available in Quartus prime to program soft core processor. [2]  
   (c) List the difference between embedded programming and application programming for embedded systems. [6]

C.O.No.3) [Comprehensive Level]

**Part C [Problem Solving Questions]**

**Answer all the Questions. Each question carries Twenty marks. (2Qx15M=30M)**

1. Hardware description language is used to design and programme FPGA for specific design.   
   (a) List the two popular HDL languages for programming FPGA?[2]  
   (b) Mention the difference between these HDL languages?[4]  
   (c) List the three popular software which allows HDL coding?[3]  
   (d) Using structural style of programming to write a HDL code for 4:1 multiplexer that can be implemented on FPGA?[6]

(C.O.No.3) [Application Level].

1. To EDA tools helps to create VLSI design in reality and also make it easy job to handle the Timing constraints and RTL design. These tools need to follow a systematic design flow of to achieve the great design. If you are a VLSI designer and you have been asked to create a prototype of the device   
   List various design modelling styles used in VLSI design?[3]     
   Explain the VLSI design flow in detail to final implementation on FPGA?[12]

(C.O.No.)[Comprehensive Level].