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PRESIDENCY UNIVERSITY BENGALURU

 SCHOOL OF ENGINEERING

 MAKE UP EXAMINATION - JULY 2024

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| **Semester : II/III** | **Date :05-JULY-2024** |
| **Course Code :EEE2015** | **Time :9:30AM-12:30PM** |
| **Course Name :** **Digital Electronics** | **Max Marks :100** |
| **Program :B.Tech**  | **Weightage :50%** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

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| **PART A** |
|  **ANSWER ANY 4 QUESTIONS 4Q X 5M=20M** |
| 1 | Define the following with example: minterm and maxterm? | (CO 2) | [Knowledge] |
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| 2 | What are Universal Gates? Why are they called so? | (CO 1) | [Knowledge] |
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| 3 | List the differences between combinational logic and sequential logic. | (CO 3) | [Knowledge] |
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| 4 | What is priority encoder? State the same with an example.  | (CO 3) | [Knowledge] |
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| 5 | What is meant by the term edge triggered and level triggered? State which triggering is used for a flip flop. | (CO 4) | [Knowledge] |
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| 6 | What is shift register? Mention the uses of shift registers. | (CO 4) | [Knowledge] |
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| **PART B** |
|  **ANSWER ANY 5 QUESTIONS 5Q X 10M=50M** |
| 7 | a. Convert the following numbersi)(163.789)10 to Octal number ii)(11001101.0101)2 to base-8 and base-4 iii)(4567)10 to base2 b) Subtract (111001)2 from (101011) using 1’s complement? | (CO 1) | [Comprehension] |
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| 8 | Simplify and implement the following SOP function.F(A,B,C,D)= ∑m(0,1,4,5,10,11,14,15) | (CO 2) | [Comprehension] |
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| 9 | Implement the following Boolean function using 8:1 multiplexerF(A,B,C.D) = Σ𝑚 (0,1,2,5,7,8,9,14,15) | (CO 3) | [Comprehension] |
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| 10 | When a LOW is on the output of each of the decoding gates in the below Figure, what is the binary code appearing on the inputs? The MSB is A3.http://guqbms.inpods.com:57953/api/v1/downloadFile?fileId=15266&tenantid=13 | (CO 3) | [Comprehension] |
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| 11 | Develop a truth table for each of the standard POS expressions: | (CO 2) | [Comprehension] |
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| 12 | Determine the Q output waveform if the inputs shown in Figure are applied to a gated D latch, which is initially RESET. | (CO 4) | [Comprehension] |
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| 13 | The waveforms in Figure are applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET. | (CO 4) | [Comprehension] |
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| **PART C** |
|  **ANSWER ANY 2 QUESTIONS 2Q X 15M=30M** |
| 14 | The J and K inputs of the J-K flip-flop are synchronous inputs because data on these inputs are transferred to the flip-flop’s output only on the triggering edge of the clock pulse. Compute the characteristic equation of JK flip flop using truth table and logic diagram. Also write the excitation table. | (CO 4) | [Application] |
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| 15 | Sketch a 3 bit asynchronous up counter and draw the timing diagram by considering a positive or negative edge triggering of a clock pulse with Ja and Ka input bit as 1. | (CO 4) | [Application] |
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| 16 | a. Determine the sum generated by the 3-bit parallel adder in Figure and show the intermediate carries when the binary numbers 101 and 011 are being added.b. Show how two 74HC283 adders can be connected to form an 8-bit parallel adder. Show output bits for the following 8-bit input numbers:A8A7A6A5A4A3A2A1 = 10111001 and B8B7B6B5B4B3B2B1 = 10011110 | (CO 3) | [Application] |
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