ROLL NO:	

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY, BENGALURU

SCHOOL OF ENGINEERING

Weightage: 20 % Max Marks: 40 Max Time: 1 hr. Monday, 24th September, 2018

TEST – 1

Odd Semester 2018-19 Course: **ECE 201 Analog Electronics** III Sem. ECE/EEE

Instruction:

(i) Read the question properly and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and Non-programmable calculators are permitted.

Part A

(3 Q x 4 M = 12 Marks)

1. State Mass-Action law. Define Diffusion current density in an n-type semiconductor with its equation.
2. Determine the values of n_0 and P_0 for Silicon with E_G = 1.12 eV at T=300 degree kelvin, if the Fermi level energy exceeds the valence band energy by 0.22 eV. Given the values of $N_V = 1.04 \times 10^{19}/cm^3$ and $N_C = 2.8 \times 10^{19}/cm^3$.
3. Define Dynamic Resistance and Transition Capacitance. Draw the static characteristics of a diode with its DC load line.

Part B

(2 Q x 8 M = 16 Marks)

4. A pure Germanium semiconductor is doped with donor impurity to the extent of 1 impurity atom for every 10^7 atom. Calculate its

   (a) Donor concentration (2 M)

   (b) Majority carrier concentration (2 M)

   (c) Minority carrier concentration (2 M)

   (d) Conductivity and Resistivity (2 M)

   Given: Total no. of atoms for Ge = $4.421 \times 10^{22}/cm^3$, Intrinsic concentration for Ge = 2.5×10^{13} atoms/cm^3, Mobilities are μ_n = 3800 cm^2/v-sec and μ_p =1800 cm^2/v-sec.

5. Consider the voltage regulator circuit of a Zener diode with V=10 V, R= 1 K Ω and break down voltage of Zener diode as 6 V. Find the zener current if (a) RL = 100 Ω and (b) RL = 9 K Ω. What are the inferences from this problem? Give the differences between Zener break down and avalanche breakdown.

Part C

(1Q x 12 M = 12 Marks)

6. (a) Explain the working of clipper and clamper circuits with diagrams and waveforms. (6 M)

   (b) Discuss the working of Common Emitter configuration of an NPN Transistor with its input and output characteristics. (6 M)

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TEST 2

Odd Semester: 2018-2019 | **Date**: 27 November 2018

Course Code: ECE 201 | **Time**: 1 Hour

Course Name: Analog Electronics | **Max Marks**: 40

Branch & Sem: ECE & EEE, III Sem | **Weightage**: 20%

Instructions:

(i) Read the question properly and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **all** the Questions. **Each** question carries **four** marks. (3x4=12)

1. Discuss the characteristics of Transistor acting as a switch.
2. Derive the stability factor S_{ICO} for emitter bias configuration.
3. Why Darlington transistors are known as super beta transistors? What is thermal runaway?

Part B

Answer **all** the Questions. **Each** question carries **eight** marks. (2x8=16)

4. (i) Draw the circuit for voltage-divider bias configuration and determine its I_{CQ} and V_{CEQ} values? (4)

(ii) Determine the operating point parameters of Collector-to-Base bias circuit with the following specifications: $R_C = 5\ K\Omega$, $R_B = 200\ K\Omega$, $R_E = 1\ K\Omega$, $V_{CC} = 15\ V$, $V_{BE} = 0.7\ V$ and gain $\beta = 165$.Also find the percentage change in value of operating point when the value of gain increases by 50 %? (4)

5. **Fig. 1** below shows a two stage CC-CB amplifier. The values of voltage gain, input and output impedance for each stage is as shown in fig 1. The values of voltage gain for both stages are mentioned for no-load condition however the input impedance and output impedance of first stage are under loaded condition. Determine

i) Loaded voltage gain for each stage. (2)
ii) Overall voltage gain of amplifier. (2)
iii) Total system voltage gain and current gain. (2)

iv) Total gain for the system if emitter-follower configuration were removed. (2)

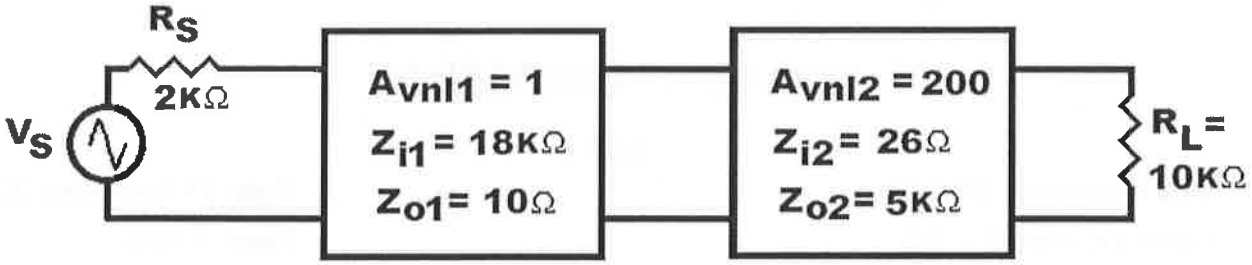

Fig. 1

Part C

Answer the Question. Question carries **twelve** marks. (1x12=12)

6. Derive the current gain and input impedance in the analysis of a transistor based amplifier using complete h-parameter model. Draw the circuit of an Emitter Follower and list its advantages.

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END TERM FINAL EXAMINATION

Odd Semester: 2018-19 | **Date**: 27 December 2018

Course Code: ECE 201 | **Time**: 2 Hours

Course Name: Analog Electronics | **Max Marks**: 80

Programme & Sem: ECE/EEE & III Sem | **Weightage**: 40%

Instructions:

(i) Read the question properly and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and Non-programmable calculators are permitted.

Part A

Answer **all** the Questions. **Each** question carries **five** marks. (4Qx5M=20)

1. Define pinch-off voltage and Saturation Drain Current (I_{DSS}) in JFET.
2. Determine the drain resistance, transconductance and amplification factor of JFET which has a drain current of 8 mA, when a drain source voltage of 5 V is applied to it with gate to source terminals shorted, i.e at zero bias. When the drain voltage is increased to 10 V, there is a small increase in drain current and the new value of drain current is 8.2 mA. When the gate source voltage is about -0.4 V, the drain current decreases to 7 mA.
3. What are the conditions needed to satisfy Barkhausen Criterion for sustained oscillations? Which oscillators are preferred for operating at high frequencies?
4. List any five advantages for introducing negative feedback in amplifiers.

Part B

Answer **all** the Questions. **Each** question carries **eight** marks. (5Qx8M=40)

5. Illustrate the working principle of N-Channel JFET with its block diagram. Discuss the significance of drain and transfer characteristics. Enumerate the applications of FET.
6. Explain self-bias configuration of N-Channel JFET and determine the DC operating point parameters by analysis with suitable expressions.
7. With the equivalent circuit of voltage-series feedback, derive the input and output resistance with feedback. Give practical examples for Voltage-Series configuration.
8. (i) Describe the working of Colpitts oscillator with circuit diagram and expression. (5)
   (ii) Derive the expression for transconductance (g_m) of JFET. (3)
9. Derive the input and output resistance with feedback for current-shunt feedback. Give a practical example for current-shunt configuration.

Part C

Answer **all** the Questions. **Each** question carries **ten** marks. (2Qx10M=20)

10. Discuss the drain and transfer characteristics of N-Channel E-MOSFET with its block schematic. Compare the characteristics of Depletion mode MOSFET with Enhancement mode MOSFET.
11. Derive the maximum efficiency in a series-fed Class A power amplifier with its block diagram. Differentiate the types of power amplifiers with their efficiencies and utilization of input cycle.