ROLL NO:	

GAIN MORE KNOWLEDGE
REACH GREATER HEIGHTS

PRESIDENCY UNIVERSITY, BENGALURU

SCHOOL OF ENGINEERING

Weightage: 20% Max Marks: 40 Max Time: 1 hr. Monday, 24th September, 2018

TEST –1

Odd Semester 2018-19 Course: **CSE 202 Digital Design** III Sem. CSE/ECE/EEE

Instruction:

(i) Read the question properly and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and Non-programmable calculators are permitted.

Part A

(2 Q x 5 M = 10 Marks)

1. Describe Positive and Negative Logic with an example.
2. State and Prove De-Morgan's Theorems.

Part B

(1 Q x 14 M = 14 Marks)

3. Find the essential prime implicants for the function
   $F(A,B,C,D)=\Sigma m(0,1,2,3,10,11,12,13,14,15)$ using Quine Mc-clusky Method

Part C

(2 Q x 8 M = 16 Marks)

4. Using K - map method, Simplify the following Boolean function
   $F(A,B,C,D) = \Sigma m(1,3,4,5,9,11,14,15) + \Sigma d(2,6,7,8)$

5. Simplify $F(A,B,C,D) = \Sigma m(0,1,2,4,5,6,8,9,10,12,13)$ using K-Map and realize the resultant expression using NAND gates only.

ROLL NO:

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TEST 2

Odd Semester: 2018-19 | **Date**: 27 November 2018

Course Code: CSE 202 | **Time**: 1 Hour

Course Name: Digital Design | **Max Marks**: 40

Branch & Sem: CSE/ECE/EEE & III Sem | **Weightage**: 20%

Instructions:

(i) Read the question properly and answer accordingly.

(ii) Question paper consists of 3 parts.

Part A

Answer the Question. Each Question carries **five** marks (2x5=10)

1. Bring out the differences between Combinational circuit and Sequential circuit with neat logic diagram
2. What are Decoders and Encoders? Write logic diagram and truth table for 2 to 4 line decoder and 4 to 2 line encoder using gates.

Part B

Answer the Question. Each Question carries **ten** marks (2x10=20)

3. What is a Multiplexer? Realize the following function using 8:1 Mux

   $F(A,B,C,D)=\Sigma m(0,1,3,7,10,11,14,15)+ \Sigma d(4,9)$

4. Design a combinational logic using appropriate range of Decoder having 4 bit inputs, the output is high when the input combination is divisible by 2 otherwise the output is low.

Part C

Answer the Question. Question carries **ten** marks (1x10=10)

5. (i) Write Verilog code for 16 : 1 Multiplexer

   (ii) List the steps followed in designing a Combinational logic circuit.

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END TERM FINAL EXAMINATION

Odd Semester: 2018-19 | **Date**: 28 December 2018

Course Code: CSE 202 | **Time**: 2 Hours

Course Name: Digital Design | **Max Marks**: 80

Programme & Sem: CSE/EEE/ECE & III Sem | **Weightage**: 40%

Instructions:

(i) Read the question properly and answer accordingly.

(ii) Question paper consists of 3 parts.

Part A

Answer the Question. Question carries **Five** marks. (1Qx5M=05)

1. Define and explain 4:1 Multiplexer and 1:4 Demultiplexer.

Part B

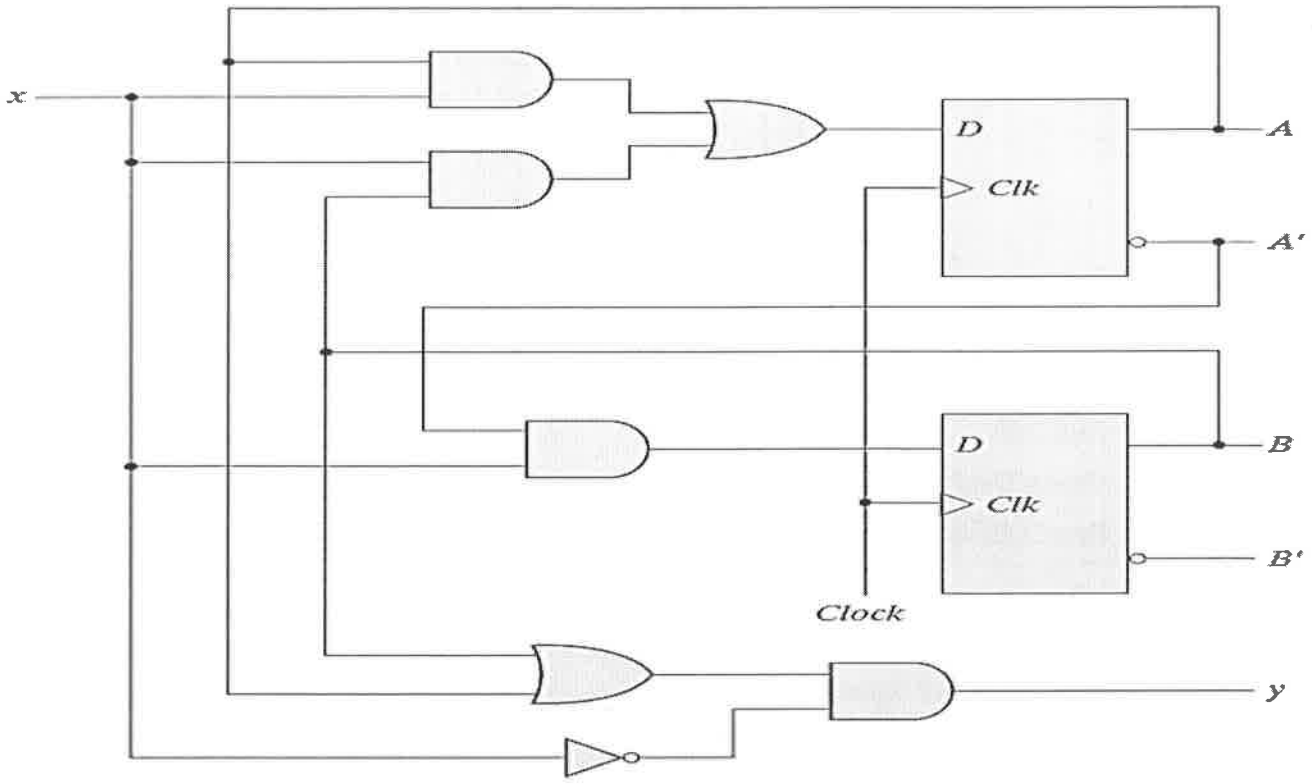
Answer **all** the Questions. **Each** question carries **ten** marks. (3Qx10M=30)

2. For the following flip-flops, write logic diagram characteristic table and excitation table:
   a) JK Flip Flop
   b) T Flip Flop
3. For the following Latches, write logic diagram and truth table
   a) SR latch
   b) D latch
4. Define Shift Register. Explain 4 modes of shift register

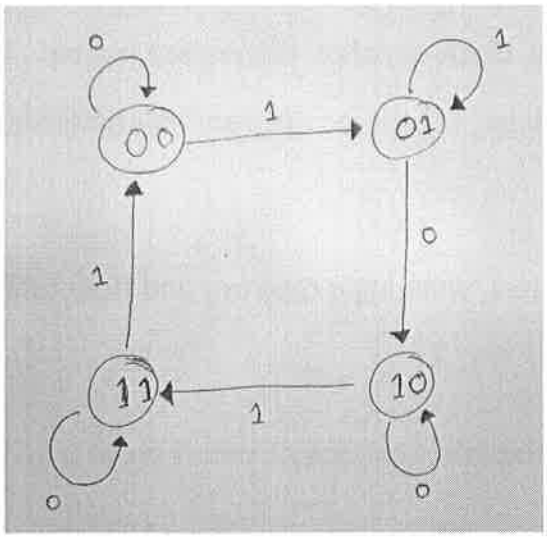
Part C

Answer **all** the Questions. **Each** question carries **fifteen** marks. (3Qx15M=45)

5. Analyze the given sequential circuit and obtain the State Transition Diagram (STD)



6. Design the sequential circuit for the given state transition for the following state transition diagrm, using JK Flip Flop.



7. With neat circuit diagram using T and D Flip Flops, explain Binary Ripple counter

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SCHOOL OF ENGINEERING — SET B

END TERM FINAL EXAMINATION

Odd Semester: 2018-19 | **Date**: 28 December 2018

Course Code: CSE 202 | **Time**: 2 Hours

Course Name: Digital Design | **Max Marks**: 80

Programme & Sem: CSE/EEE/ECE & III Sem | **Weightage**: 40%

Instructions:

(i) Read the question properly and answer accordingly.

(ii) Question paper consists of 3 parts.

Part A

Answer the Question. Question carries **five** marks. (1Qx5M=05)

1. Design 32:1 Multiplexer using only 4:1 and 2:1 MUX.

Part B

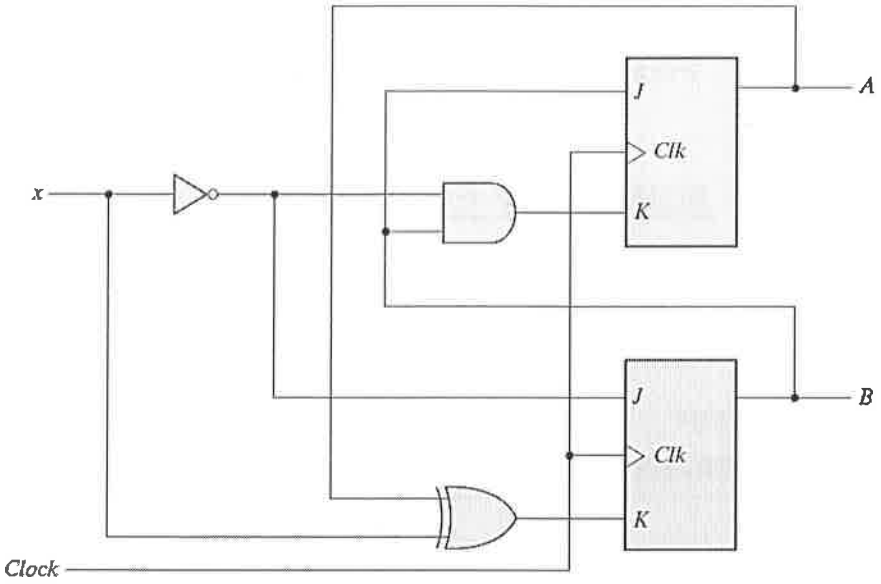
Answer **all** the Questions. **Each** question carries **ten** marks. (3Qx10M=30)

2. Explain SR and D flip-flops, with logic diagram, characteristic table and excitation table:
3. Design SR and D latch using NAND gates along with Function table
4. With neat logic diagram, explain Ring and Johnson counter using IC 7495 with truth table.

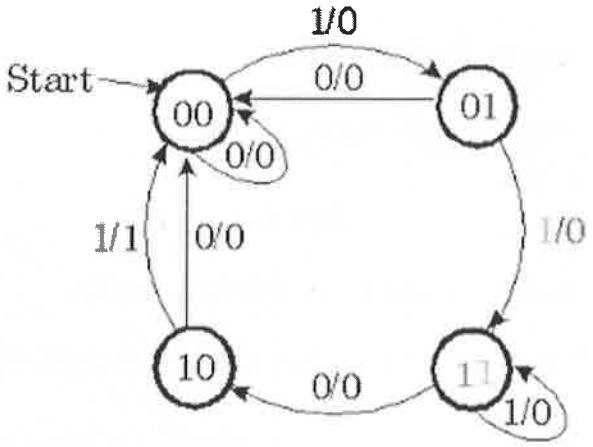
Part C

Answer **all** the Questions. **Each** question carries **fifteen** marks. (3Qx15M=45)

5. Analyze the given sequential circuit and obtain the State Transition Diagram (STD)



6. Design the sequential circuit for the given state transition diagram using D Flip flop



7. Write Verilog code for the following:
   a) D Flip Flop
   b) Mod 8 up counter.