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PRESIDENCY UNIVERSITY BENGALURU

**SET-A**

SCHOOL OF ENGINEERING

**END TERM EXAMINATION – MAY/JUN 2024**

**Semester :** Semester II - 2023

**Course Code :** ECE2002\_v02

**Course Name :** - Digital Electronics

**Program :** B.Tech. Electronics and Communication Engineering

**Date :** June 20 2024

**Time :** 1:00 PM - 4:00 PM

# Max Marks : 100

**Weightage :** 50%

# Instructions:

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

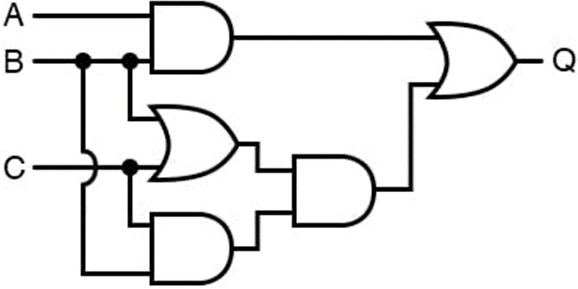
**PART A**

**ANSWER ANY THREE QUESTIONS (3 Q X 5 M = 15 M)**

1. Lohit uses a three input AND gate to design a digital circuit. How many input combinations will lead to a low output? Support your answer with the help of a truth table.

(CO1) [Knowledge]

1. A logic diagram containing basic gates is given below. Write the expression that will be obtained at Q.



(CO1) [Knowledge]

1. Sequential circuits are digital circuits that store and use the previous state information to determine their next state. Unlike combinational circuits, which only depend on the current input values to produce outputs, sequential circuits depend on both the current inputs and the previous state stored in memory elements. Two such sequential circuits are latch and flip flop. Write at least 5 differences between a latch and a flip flop.

(CO4) [Knowledge]

1. A MUX finds its application in data routing, data selection, address decoding as well as to implement various logic functions and Boolean expressions. Implement the Boolean expression f=∑m(0,1,3,5,7,10,12,14) using 8:1 MUX using Map Entered Variable technique.

(CO3) [Knowledge]

1. With the help of truth table, illustrate the number of clock cycles required by Serial Input Serial Output and Parallel Input Parallel Output shift registers. Highlight the major differences in logic diagram of SISO and PIPO registers.

(CO4) [Knowledge]

**PART B**

**ANSWER ANY TWO QUESTIONS (2 Q X 20 M = 40 M)**

1. Divya intends to reduce the number of gates in a given circuit, thereby simplifying a complex circuit reducing the cost, size and area of the integrated circuit. Divya is given an expression F=∑(1,2,3,4,5,6,7,8,9,10,11,12,13,14,15). Minimize this expression and implement. She finds that she is not left with any basic gates to use. In the rack she finds a bunch of universal gates whose output is HIGH if at least one of the inputs is HIGH. This universal gate has 2 inputs and 1 output as per its pin configuration. Implement the simplified expression using the universal gates described above.

(CO2) [Comprehension]

1. A combinational circuit has ‘n’ input lines and a maximum of output lines, that outputs min terms of ‘n’ input variables lines. Explain the specified circuit without enable input. Explain the disadvantage of this circuit.

(CO3) [Comprehension]

1. Almost all traffic signals carry a down counter to indicate the remaining time before red/green lights are turned off. Design a 3-bit down counter using SR Flipflop.

(CO4) [Comprehension]

**PART C**

**ANSWER ANY THREE QUESTIONS (3 Q X 15 M = 45 M)**

1. Flip flops and latches are used as data storage elements. In case of T flip flop, if the T input is high, the T flip flop changes state ("toggles") whenever the clock input is strobed. If the T input is low, the flip flop holds the previous value. Draw the logic symbol and circuit diagram, characteristic table and equation, excitation table for this flip flop.

(CO4) [Application]

1. Students are given two tasks related to combinational circuits.

Task 1: Perform the addition of two input bits: A and B, that represent the two significant bits to be added and produce two outputs.

Task 2: Perform the addition of three input bits: A and B, that represent the two significant bits to be added, and a Cin input that is a carry-in from the previous significant position.

Draw the logic diagram using the NAND gates of these circuits and write its truth table. Include Kmap simplification to justify the output expressions thus obtained.

(CO3) [Application]

1. Boolean algebra is subject to certain rules which may be applied in the task of simplifying (reducing) expressions. By being able to algebraically reduce Boolean expressions, it allows us to build equivalent logic circuits using fewer components. Simplify and build a circuit for the expression Y = AB’+A(B+C)’+B(B+C)’ using basic gates.

(CO1) [Application]

1. Find the Boolean expression in the standard sum of product (SOP) from the given truth table and simplify the expression using Kmap and implement using NAND gates

|  |  |
| --- | --- |
| **Inputs** | **Outputs** |
| X Y Z | F |
| 0 0 0 | 1 |
| 0 0 1 | 1 |
| 0 1 0 | 0 |
| 0 1 1 | 1 |
| 1 0 0 | 0 |
| 1 0 1 | 0 |
| 1 1 0 | 0 |
| 1 1 1 | 1 |

(CO2) [Application]