|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Roll No |  |  |  |  |  |  |  |  |  |  |  |



PRESIDENCY UNIVERSITY BENGALURU

 **SET-A**

SCHOOL OF ENGINEERING

**END TERM EXAMINATION – MAY/JUNE 2024**

**Semester :** Semester II - 2023

**Course Code :** ECE2007

**Course Name :** ECE2007 - Digital Design

**Program :** B.Tech. Computer Science and Engineering

**Date :** June 20, 2024

**Time :** 1:00 PM - 4:00 PM

**Max Marks :** 100

**Weightage :** 50%

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

**PART A**

**ANSWER ANY THREE QUESTIONS (3 Q X 5 M = 15 M)**

* 1. NAND and NOR gates are universal gates, which means that any other logic gates can be implemented using them. **Draw the XOR logic circuit using four NAND gates:**

(CO1) [Knowledge]

* 1. Multiplexer is a combinational circuit used as a parallel-to-serial converter, which has multiple input lines and single output line. **Write the truth table and derive the AND gate logic using 2x1 MUX:**

(CO2) [Knowledge]

* 1. Decoders is a combinational circuit, it is used when an analog signal needs to be understood by digital circuits. With the help of truth-table, **design a Full Subtractor using a 3-8 line Decoder**:

(CO2) [Knowledge]

* 1. Multiplexer is used for Data selection. **Draw the 4x1 Multiplexer using basic gates**, which has 4 input data lines and 1 output line with 2 selection lines:

(CO2) [Knowledge]

* 1. The shift register is an essential component in digital circuits for efficient data storage and manipulation, which can shift the binary bits either right or left. **Draw the 4-bit Serial-In-Parallel-Out (SIPO) shift register:**

(CO3) [Knowledge]

**PART B**

**ANSWER ANY TWO QUESTIONS (2 Q X 20 M = 40 M)**

* 1. Priority Encoder circuit play essential roles in digital communication by efficiently converting input data into encoded output addresses. **Design a 4 into 2 line Priority Encoder:**

(CO2) [Comprehension]

* 1. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems. **For a JK flipflop, draw the logic symbol, circuit diagram and derive the characteristic table, characteristic equation (Next State equation) and excitation table:**

(CO3) [Comprehension]

* 1. In general, all automatic traffic signals use a down counter to indicate the remaining time before red/green lights are turned off. **Using a state-table and K-maps, design a 3-bit counter using JK flip-flops to count the number decremented from 7 to 0 in binary form:**

(CO3) [Comprehension]

**PART C**

**ANSWER ANY THREE QUESTIONS (3 Q X 15 M = 45 M)**

* 1. Given SoP Boolean expression is

**F = ( W' X' Y' Z' ) + ( W Y' Z' ) + ( X' Y Z' ) + ( W' X Y Z ) +( X Y' Z ).**

* + 1. **Convert Standard SoP into Canonical SoP form.**
		2. Using K-Map find the **simplified PoS** expression and implement **using NOR gate only**?

(CO1) [Application]

* 1. A student wants to design a digital logic switching function which is described by the following Boolean Function. The function can be expressed algebraically using binary variables, constants (0 and 1), and logical operation symbols. **F(A,B,C,D)=⅀m(1,3,4,11,12,13,14,15)**. But he has been provided with 8x1 MUX and other minimum gates. With the help of a truth-table, guide the student to **design the Boolean function using MUX:**

(CO2) [Application]

* 1. Mr. Rao intends to to use a K-map to minimize the Boolean expression

**f=π M (0,1,2,4,7,8,9,10,12) + d(3,6,13,15)**. Help him to implement the expression **with minimum number of sum terms using NOR gates only:**

(CO2) [Application]

* 1. The designer can design a Full adder using two Half Adders and one basic gate. In general, a Half Adder circuit has an Ex-OR gate & AND gate. From the Full Adder truth table, using K-Map derive the needed expression and **design a Full Adder circuit using Half Adders and one OR gate:**

(CO2) [Application]