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PRESIDENCY UNIVERSITY BENGALURU

**SET-B**

SCHOOL OF ENGINEERING

**END TERM EXAMINATION – MAY/JUN 2024**

**Semester :** Semester II - 2023

**Course Code :** ECE2007

**Course Name :** Digital Design

**Program :** B.Tech. Computer Science and Engineering

**Date :** June 20, 2024

**Time :** 1:00 PM - 4:00 PM

# Max Marks : 100

**Weightage :** 50%

# Instructions:

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

**PART A**

**ANSWER ANY THREE QUESTIONS (3 Q X 5 M = 15 M)**

1. NAND and NOR gates are universal gates, which means that any other logic gates can be implemented using them. **Draw the XNOR logic circuit using five NAND gates:**

(CO1) [Knowledge]

1. Multiplexer is a combinational circuit used as a parallel-to-serial converter, which has multiple input lines and single output line. **Write the truth table and derive the OR gate logic using 2x1 MUX:**

(CO2) [Knowledge]

1. Decoders is a combinational circuit, it is used to convert an analog signal into digital data, which can be processed by a computer. With the help of truth-table, **design a Full Adder using a 3-8 line Decoder:**

(CO2) [Knowledge]

1. De-multiplexer is used for Data distribution. **Draw the 1x4 De-Multiplexer using basic gates**, which has 1 input data line and 4 output lines with 2 selection lines:

(CO2) [Knowledge]

1. A shift register is a group of interconnected flip-flops that can store and shift binary data both inside and outside the flip-flops. **Draw the 4-bit Serial-In-Serial-Out (SISO) shift register:**

(CO3) [Knowledge]

**PART B**

**ANSWER ANY TWO QUESTIONS (2 Q X 20 M = 40 M)**

1. Priority Encoder circuit is used, when multiple inputs are active simultaneously, the output corresponds only to the input with the highest designated priority. **Design a 4 into 2 line Priority Encoder:**

(CO2) [Comprehension]

1. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems. **For a SR flipflop, draw the logic symbol, circuit diagram and derive the characteristic table, characteristic equation (Next State equation), and excitation table:**

(CO3) [Comprehension]

1. In many domestic application (like Digital Clock, Timers…) Up counter logic circuits are used frequently. **Using a state-table and K-maps, design a 3-bit counter using JK flip-flops to count the decimal number from 0 to 7 in binary form:**

(CO3) [Comprehension]

**PART C**

**ANSWER ANY THREE QUESTIONS (3 Q X 15 M = 45 M)**

1. Given PoS Boolean expression is **F = ( B + C’ + D’ ) (A’ + B’ + C + D) ( A + B’ + C’ + D’ )**. i)**Convert Standard PoS into Canonical PoS.**

ii)Using K-Map, find the **simplified SoP** expression and implement **using NAND gate only**?

(CO1) [Application]

1. A Boolean function is a mathematical function that takes binary inputs and produces a binary output. Which can be implemented in many ways. A student, he has been provided with only 8x1 MUX and other minimum gates. With the help of a truth-table, guide the student to **design the Boolean function F(A,B,C,D)=⅀m(1,3,4,11,12,13,14,15)**. **using MUX:**

(CO2) [Application]

1. Mr. Joe intends to use a K-map to minimize the Boolean expression

**f=∑ m(0,1,2,4,7,8,9,10,12) + d(3,6,13,15)**. Help him to implement the expression **with minimum number of product terms using NAND gates only:**

(CO2) [Application]

1. The designer can design a Full Adder using two Half Adders and one basic gate. Usually, a Half Adder circuit has an Ex-OR gate & an AND gate. From the Full Adder truth table, using K-Map derive the needed equation and **design a Full Adder circuit using Half Adders and one OR gate:**

(CO2) [Application]