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PRESIDENCY UNIVERSITY BENGALURU

**SET-A**

SCHOOL OF ENGINEERING

**END TERM EXAMINATION – MAY/JUNE 2024**

**Semester :** Semester IV - 2022

**Course Code :** ECE3003

**Course Name :** - Microprocessor Programming and Interfacing

**Program :** B.Tech.

**Date :** June 14, 2024

**Time :** 9:30 AM -12:30 PM

**Max Marks :** 100

**Weightage :** 50%

# Instructions:

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

**PART A**

**ANSWER ANY FIVE QUESTIONS (5 Q X 4 M = 20 M)**

1. State difference between carry and Auxillary carry for 8 bit and 16 bit operation. Explain with suitable example.

(CO1) [Knowledge]

1. Different modes of addressing are used by 8086 Microprocessor. Identify the addressing modes for the following instructions. i) MOV DL, [BX+SI+

50h] ii) MOV AL, [BX+78h]

(CO2) [Knowledge]

1. 8086 incorporates pipelined architecture with a dedicated BIU. What is the size of instruction queue in 8086. How does it affect the performance of the processor , explain in context with EU and BIU of 8086

(CO3) [Knowledge]

1. Form the Control Word in Hex for configuring the 8255 in simple I/O mode with the details of ports as indicated below:

Port CL = Input Port CU = Output

Port B = Input in Mode 0 Port A = Output in Mode 1

(CO3) [Knowledge]

1. What is the function of 8288 bus controller ? How does it help in Memory / IO device read and write operations.

(CO3) [Knowledge]

1. What is the total Memory addressing capacity of the following microprocessors i) 8086 ii) 80186 iii) 80286 iv) 80486

(CO4) [Knowledge]

1. An Instruction executes in 5 different stages for an intel 8086/80186 processor. What are the different states in the execution cycle of a microprocessor.

(CO4) [Knowledge]

**PART B**

**ANSWER ANY FOUR QUESTIONS (4 Q X 10 M = 40 M)**

1. Assembly languages program contain mnemonic codes that specify what the processor should do. Write an ALP to find odd or even for a given number.

(CO2) [Comprehension]

1. Microprocessor has ALU, which perform arithmetic and logical operations. During these operations, the status of the result is stored in the flag register, which is a 16 bits register. With suitable example, explain how this flag register bits are affected after each operation.

(CO2) [Comprehension]

1. The 8255 simple I/O mode is used to interface a number of input devices like keypads and output devices like LEDs. In order to configure their operation, the control register of 8255 has to be programmed,

a. Write the BSR control words for the following cases:

* 1. PC1 to be set
  2. PC6 to be reset
  3. PC5 to be set
  4. PC2 to be reset

(CO3) [Comprehension]

1. 8255 is designed by **Intel** to increase the number of ports for I/O interfacing of the microprocessor. Explain the role and function of each major component of 8255, including the Control Register, Group A and Group B ports.

(CO3) [Comprehension]

1. Write a Delay Program to generate a Delay of 1 second assuming the clock frequency to be 12 Mhz. Explain each instruction in detail with calculations of T -States

(CO4) [Comprehension]

1. What are different types of Memories that can be interfaced with the microprocessor. Explain each memory type in detail and usage in real world.

(CO4) [Comprehension]

**PART C**

**ANSWER ANY TWO QUESTIONS (2 Q X 20 M = 40 M)**

1. The 16-bit segment register values are combined with an offset to get the physical addresses in an 8086 processor. Given that the DS contains 1AAAh and the offset address is 7777h, then calculate the following addresses Also, Given that the SS contains 2FFFh and the SP address is EEEEh, then calculate the following addresses
2. Lower Range address in the Data Segment and Stack segment
3. Upper Range address in the Data Segment and Stack segment
4. Logical address in the Data Segment and Stack segment
5. Physical address in the Data Segment and Stack segment

(CO2) [Application]

1. Explain the process of interrupt handling in the 8086 microprocessor, covering both hardware and software aspects. Discuss the different types of interrupts supported by the 8086, their priority levels, and the steps involved in handling an interrupt. Additionally, describe how interrupt vectors are used in the interrupt handling process, and provide examples of real-world scenarios where interrupt handling plays a crucial role in system functionality.

(CO3) [Application]

1. In Pipelined architecture of a microprocessor, the instructions are exected parallelly. Elaborately explain the concept of a pipelined processor executing 7 Instructions in queue. The 3rd 4th and 6th instruction has 2, 3 and 3 Execute states respectively. Compare the timing of this processor with a processor that does not incorporate pipelining.

(CO4) [Application]