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PRESIDENCY UNIVERSITY BENGALURU

**SET-B**

SCHOOL OF ENGINEERING

**END TERM EXAMINATION – MAY/JUNE 2024**

**Semester :** Semester VI - 2021

**Course Code :** ECE3044

**Course Name :** - IC Fabrication Technology

**Program :** B.Tech.

**Date :** Jun 19, 2024

**Time :** 1:00 PM - 4:00 PM

**Max Marks :** 100

**Weightage :** 50%

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

**PART A**

**ANSWER ANY THREE QUESTIONS (3 Q X 5 M = 15 M)**

* 1. Chemical Vapor Deposition technology produces high-quality material building blocks that underpin various fields of applications. Apparatus in which the substrate is brought into contact with the solution. Identify the apparatus used for this and explain in brief using required diagram.

(CO2,CO1) [Knowledge]

* 1. VLSI technology encompasses both analog and digital design aspects. While the analog circuits excel in processing continuous signals with precision, digital circuits excel in performing complex computations & logical operations. What are the factors that have led to the evolution and enhancement of VLSI Integrated Circuits?

(CO2,CO1) [Knowledge]

* 1. SiO2 is an oxide of silicon with a chemical name silicon dioxide. Silicon oxide is patterned on a substrate using . Explain the technique.

(CO3) [Knowledge]

* 1. A dopant is a small amount of a substance added to a material to alter its physical properties. These are introduced in the active areas of silicon during manufacturing IC by using which process? Explain using example.

(CO4) [Knowledge]

* 1. In Federal Standard 209 (A to D) of the USA, the number of particles equal to and greater than 0.5mm is measured in one cubic foot of air, and this count is used to classify the cleanroom. Define Clean Room and mention the standards.

(CO3,CO4) [Knowledge]

**PART B**

**ANSWER ANY TWO QUESTIONS (2 Q X 20 M = 40 M)**

* 1. Diffusion is the net movement of anything (for example, atoms, ions, molecules, energy) generally from a region of higher concentration to a region of lower concentration.Interpret 2 mechanisms to loose kinetic energy of the ions after getting implanted on the wafer. Verify using relationship between stopping power with respect to ion velocity.

(CO1,CO2) [Comprehension]

* 1. The method offfers high resolution because of small wavelength of electrons less than equal to 0.1nm for 10-50eV.
     1. Analyze the menthod and mention the advantages of this technique.
     2. If diameter of x-ray source is 4.85 mm and the radial distance is given by 5.7mm. Find the ratio of penumbral effect (§) by run out.

(CO3) [Comprehension]

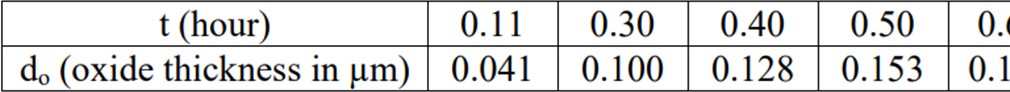
* 1. The deposition of an overlayer on a crystalline substrate, where the overlayer is in registry with the substrate used for high purity layer growth. Analyze the method and explain any one of the types in detail.

(CO4) [Comprehension]

**PART C**

**ANSWER ANY THREE QUESTIONS (3 Q X 15 M = 45 M)**

* 1. In Wet oxidation of silicon at 950 deg Celsius, the following data are obtained:



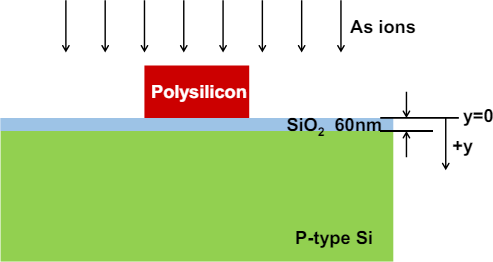
Show how to graphically show the linear and parabolic rate constants from these experimental data. Assume that τ = 0 for wet oxidation.

(CO4) [Application]

* 1. Fabrication in VLSI(Very Large Scale Integration) refers to the process of physically realizing the IC chip which was designed using software. Explain NMOS Fabrication steps using suitable diagram.

(CO3) [Application]

* 1. Consider the following cross section that is to be doped with Arsenic using ion implantation to form the source/drain regions. Assume the Si substrate is initially doped with B with a uniform concentration of 10^16 cm-3 .



1. Assume that the SiO2 and polysilicon layers have the same ion stopping power as Si, and that SiO2 thickness is 60 nm. What are the ion implantation dose and energy required to achieve a peak concentration of 10^19 cm-3 of As at the SiO2 and Si interface in the source/drain regions (i.e., y = 60 nm)?
2. Calculate the junction depth of the source/drain regions.

(CO4,CO3) [Application]

* 1. The killing defect density is responsible for yield loss and depends on the design rule or size of the device on a chip. This is because when the design rule becomes smaller, a smaller particle can contribute to yield loss. For a 16M DRAM chip, the design rule is 0.5 µm, chip size is 1.4 cm2 , and killing defect size is 0.18 µm. Due to contamination that occurs in a cleanroom, the wafer defect density measured at size 0.3 µm increases fivefold from 0.2 D/cm2 to 1.0 D/cm2 . Using the relationship DA Y =e^-(DA) where D is the defect density and A is the chip area, calculate the yield loss of a 16M DRAM wafer due to the increase in the aforementioned defect density assuming that the defect density is roughly inversely proportional to the defect size to the second power.

(CO3,CO4) [Application]