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PRESIDENCY UNIVERSITY BENGALURU

 **SET-A**

SCHOOL OF ENGINEERING

**END TERM EXAMINATION – MAY/JUNE 2024**

**Semester :** Semester VI - 2021

**Course Code :** ECE3046

**Course Name :** Low Power VLSI Design

**Program :** B.Tech. Electronics and Communication Engineering

**Date :** June 19, 2024

**Time :** 1:00 PM - 4:00 PM

# Max Marks : 100

**Weightage :** 50%

# Instructions:

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

**PART A**

**ANSWER ANY THREE QUESTIONS (3 Q X 5 M = 15 M)**

1. The body effect technique is used in Variable –Threshold CMOS(VTMOS). Describe VTCMOS.

(CO1) [Knowledge]

1. Gate-level simulation is an important aspect of VLSI design flow. Write short notes on GLS.

(CO2) [Knowledge]

1. The various operator is used in local restructuring for designing the low-power circuit. List out the transformation operators in local restructuring.

(CO3,CO2) [Knowledge]

1. Skew minimization is based on adjusting the interconnect lengths and widths. Illustrate skew, zero skew and tolerable skew.

(CO3,CO4) [Knowledge]

1. The NMOS and PMOS size is changed to adjust the rise and fall time of the circuit. Perform transistor sizing of 4-input CMOS NOR gate.

(CO5) [Knowledge]

**PART B**

**ANSWER ANY TWO QUESTIONS (2 Q X 20 M = 40 M)**

1. . (i) The capacitance is one of the important parameters of average power dissipation. Explain capacitive power dissipation.

(ii) The glitch power dissipation is reduced by using the pipelining technique. Illustrate the importance of pipelines in low-power design with an example.

(CO3,CO2) [Comprehension]

1. The low-power technique is implemented at the circuit level. (i) Design any precomputation logic circuit and describe it. (ii) Discuss the importance of signal gating in low-power VLSI design.

(CO4,CO3) [Comprehension]

1. Performance management is an important issue in architecture-level management. Explain power and performance management.

(CO5,CO4) [Comprehension]

**PART C**

**ANSWER ANY THREE QUESTIONS (3 Q X 15 M = 45 M)**

1. The power is dissipated when a direct path forms between the power supply and ground. Describe (i) Reverse diode leakage current (ii) Subthreshold leakage current.

(CO3,CO2,CO1) [Application]

1. The Latch and Flip flop are the first and last elements of any circuit. Describe the special FF and Latch for lower power design.

(CO4,CO3) [Application]

1. Many techniques have been devoted to the power efficiency of clock generation and distribution. Explain (i) Clock gating. (ii) Reduced swing clock.

(CO4) [Application]

1. The most popular gate-level analysis is based on the so-called event-driven logic simulation. Describe it.

(CO5) [Application]