Roll No											

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF INFORMATION SCIENCE
END TERM EXAMINATION - AUGUST 2024

Semester : IV (DCET)	**Date :08-08-2024**
Course Code :CSE2009	**Time : 9:30 AM to 12.30 PM**
Course Name : Computer Organization and Architecture	**Max Marks : 100**
Program : B.Tech CSE - (DCET)	**Weightage : 50%**

Instructions:

(i) Read all questions carefully and answer accordingly.
(ii) Question paper consists of 3 parts.
(iii) Scientific and non-programmable calculator are permitted.
(iv) Do not write any information on the question paper other than Roll Number.

PART A			
	ANSWER ANY 5 QUESTIONS		**5Q X 2M=10M**
1	Distinguish between the CISC and RISC processor.	(CO 1)	[Application]
2	Distinguish between the Static RAM and Dynamic RAM.	(CO 3)	[Application]
3	Draw the flowchart of Memory Hierarchy in Computers.	(CO 3)	[Knowledge]
4	Derive the processor execution time equation for a computer system.	(CO 1)	[Application]
5	Depict the flowchart of Programmed I/O Communication technique.	(CO 1)	[Knowledge]
6	Outline the control sequence for the instruction **SUB R1, R2, R3** in Single Bus architecture.	(CO 2)	[Application]
7	Distinguish between the MAR and MDR in Computer Architecture.	(CO 3)	[Application]

PART B			
	ANSWER ANY 5 QUESTIONS		**5Q X 10M=50M**
8	Explain in detail about the connection between memory and processor of a computer.	(CO 1)	[Comprehension]
9	Discuss about the various addressing modes of a computer with example.	(CO 1)	[Comprehension]
10	Suppose main memory consists of 32 blocks of 4 words each and cache consists of 4 blocks. How many bits required for main memory address? How many bits are there in each of Tag, block/set and word fields for different mapping techniques?	(CO 3)	[Application]

11	Derive the equation for Carry Look Ahead adder for 4 bits with necessary diagrams.	(CO 2)	[Application]
12	Perform the division using Restoration Algorithm for 15 by 9.	(CO2)	[Application]
13	Demonstrate the importance of DMA in Computer architecture with block diagram.	(CO3)	[Application]
14	Explain the architecture of Multiple Bus Architecture with suitable diagram.	(CO 3)	[Comprehension]

PART C			
	ANSWER ANY 2 QUESTIONS		**2Q X 20M=40M**
14	Evaluate the 5-bit signed number addition by indicating the overflow values for the following i. (-12) + (-10) ii. (-9) – (-13) iii. (-11) + (-8) iv. (-9) – (-8) v. (+14)+(-7)	(CO 2)	[Application]
15	i. Illustrate the control sequence for the instruction **ADD (R2), R1** for the single bus architecture with diagram. ii. Demonstrate the concept of instruction hazard in pipelining with 3 instructions and the 1st instruction is delayed at fetch phase for a period of 3 cycles (from 2nd cycle to 4th cycle).	(CO 3)	[Application]
16	i. Making use of Non-Restoration Method, divide the value of 14 by 5. ii. Multiply the value of (+34) and (+43) using the Booth's algorithm.	(CO 2)	[Application]