Roll No												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

END TERM EXAMINATION AUGUST-2024

Even Semester : 2023-2024
Course Code : ECE5010
Course Name : Design For Testability
Program & Sem: M.Tech (ESV) & II

Date :21 / 08 / 2024
Time: 09:30 AM to 12:30 PM
Max Marks: 100
Weightage: 50%

Instructions:

(i) Read the all questions carefully and answer accordingly. All parts are compulsory.
(ii) Do not write any information on the question paper other than Roll Number.

Part A [Memory Recall Questions]

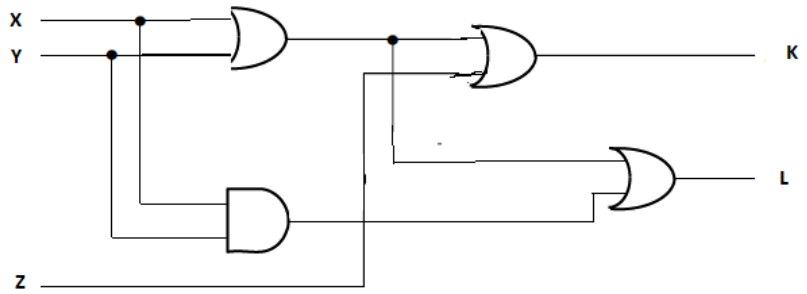
Answer any 3 Questions. Each question carries 5 marks. (3Qx 5M= 15M)

1. Write the advantages and Disadvantages of Traditional Test Methods: [5M] (C.O.No.1) [Knowledge]
2. Draw the schematic sequential circuit with scan path: [5M] (C.O.No.2) [Knowledge]
3. Draw the Multiplexers block diagram with controllability and observability test point: [5M] (C.O.No.2) [Knowledge]
4. Draw the CUT with JTAG standard. [5M] (C.O.No 3) [Knowledge]
5. Define the following i) Fault Masking ii) Signature Analysis [5M] (C.O.No.3) [Knowledge]

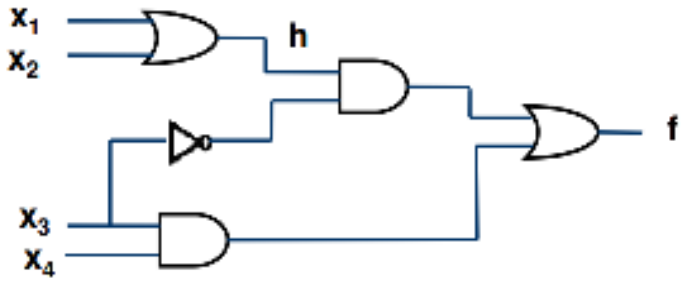
Part B [Thought Provoking Questions]

Answer any 4 Questions. Each question carries 10 marks. (4Qx10M=40M)

6. Explain the following i) Basic Architecture of BIST ii) schematic architecture of Boundary-Scan Chip [10M](C.O.No.4) [Comprehension]
7. Explain about CMOS / NMOS Chip Fabrication Process [10M](C.O.No.1) [Comprehension]
8. Calculate the standard Combinational Controllability and Observability measures for the given circuit? [10M](C.O.No.1) [Comprehension]



9 . Generate tests for the given below circuit using ATPG: [10M](C.O.No.2) [Comprehension]



10.Explain the following i) serial fault simulation ii) Fault dropping ii) Fault collapsing [10M](C.O.No.3) [Comprehension]

11.Draw and Describe a Scan Cell Unit: [10M](C.O.No.3) [Comprehension]

Part C [Problem Solving Questions]

Answer any 3 Questions. Each question carries 15 marks. (3Qx15M=45M)

12.Write the general SCOAP Combinational Observability and Combinational Controllability (ZERO & ONE) calculation rule for AND and OR gate logic: Also compute testability Measures for the following gates i) Three input AND ii) Three input OR iii) Two input ExOR [15M](C.O.No.2) [Comprehension]

13.State and explain bridge fault: [15M](C.O.No.3) [Comprehension]

14.Explain parallel fault simulation with example: [15M](C.O.No.4) [Comprehension]

15.Using LFSR, describe the Signature Analysis: [15M](C.O.No.4)[Comprehension]

16.Why is Automated Test Equipment (ATE) important? Write down the common issues and problems with ATE? [15M](C.O.No.2) [Comprehension]