PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

END TERM EXAMINATION

Even Semester:

Course Code: ECE5016

Course Name: IC Fabrication Technology

Program & Sem: M.Tech, 2nd Semester

Date: 19/ 08 / 2024

Time: 09:30 AM to 12:30 PM

Max Marks: 100

Weightage: 50%

Instructions:
(i) *Read the all questions carefully and answer accordingly. All parts are compulsory.*
(ii) *Do not write any information on the question paper other than Roll Number.*

Part A [Memory Recall Questions]

Answer any 2 Questions. Each question carries 10 marks.   **(2Qx 10M= 20M)**

1. A semiconductor bar of length 2 mm with intrinsic carrier concentration of 10^{13} per cm-^{3} is uniformly doped with donors at a concentration of $2*10^{13}$ cm^{-3} and acceptors at a concentration of $2*10^{13}$ cm^{-3}. If $D_n = 26\ cm^2/s$ and $D_p = 52\ cm^2/s$, calculate the electron and hole drift current densities for an applied voltage of *5 V*. In this semiconductor, electrons are in the ohmic regime for fields less than 10^5 *V/cm*, but travel with a saturation velocity of *10^8 cm/s* for fields above that. For holes, they are ohmic below 10^4 *V/cm*, and travel with a saturation velocity of 10^5 *cm/s* above that field. What are the electron and hole diffusion current densities in the middle of the bar? (Assume *T = 300 K*.)

2. In a p$^+$n diode reverse biased at *5* V, the generated capacitance is 20 pF. If the doping of the p side is doubled and the bias is change to 20 V, what will be the change in capacitance? If now the bias is changed to 100 V, then what will be the change?

3. Calculate V_T of a Si n-channel MOSFET with $\varphi_{ms} = -0.25\ V$, gate oxide thickness of $100\ nm$, $N_A = 10^{17}$ per cm^3, and oxide charge density $5 \times 10^{18}\ C/cm^2$ for a substrate bias of $-2\ V$. ($Q_D = 6 \times 10^{-8}\ C/_{cm^2}$). If the channel mobility is $\mu_n = 250\ cm^2/V - s$, then what will be the drive current for a 50-nm channel MOSFET with gate bias at *2 V* working at saturation region? The length of the MOSFET is *2 μm*.

Part B [Thought Provoking Questions]

Answer any 2 Questions. Each question carries 15 marks.   **(2Qx15M = 30M)**

4. Consider a PN junction where the space-charge region extends from $-x_p$ to $+x_n$ with acceptor and donor ion concentrations N_D and N_A. Using Poisson's equation, derive the expression for built-in potential V_{bi}. Hence, find the total width W of the junction.

5. Silicon is the most widely used element in the semiconductor industry, which is available abundantly on the earth's crust.

(a) Discuss the process of purification of silicon to obtain a semiconductor grade silicon.
(b) The Czochralski's process involves melting and freezing silicon to which a dopant is added. Discuss the Czochralski's process in details.

6. A cleanroom or clean room is an engineered space that maintains a very low concentration of airborne particulates.
(a) Mention the specifications of different ISO class cleanrooms.
(b) Mention the cleanroom materials with emphasis on water and chemicals.
(c) Describe the possible contaminant types in a cleanroom.

Part C [Problem Solving Questions]

Answer any 2 Questions. Each question carries 25 marks.   (2Qx25M=50M)

7. The MOSFET consists of an insulating oxide layer sandwiched between a doped semiconductor and a metal layer. For such a MOSFET (3+5+2+15)
        (a) Mention the four different operating conditions.
        (b) Draw the energy band diagrams for these conditions with proper labelling.
        (c) Mention the phenomenon of band-bending for the appropriate layer under the relevant conditions
        (d) Derive an expression for depletion width at inversion.

8. The process of IC fabrication involves several steps starting from highly purified silicon wafer. Mention the steps with a brief description of each of them. (6+19)

9. Of the different types of FETs, the JFET, in spite of its drawbacks, has advantages like simpler manufacturing process and more robustness towards static charges. Explain the phenomenon of pinch-off voltage V_D and derive an expression for drain saturation current I_D in terms of V_D for such a device. (5 + 20)