Roll No												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

END TERM EXAMINATION AUGUST-2024

Even Semester:
Course Code: ECE6003
Course Name: Low Power VLSI Design
Program & Sem: M.Tech, 2nd Sem

Date: 20 /08 /2024
Time: 09:30 AM to 12:30 PM
Max Marks: 100
Weightage: 50%

Instructions:
(i) Read the all questions carefully and answer accordingly. All parts are compulsory.
(ii) Do not write any information on the question paper other than Roll Number.

Part A [Memory Recall Questions]

Answer any 3 Questions. Each question carries 5 marks. (3Qx 5M= 15M)

1. Explain the need for low power consumption in VLSI designs. [5M] (C.O.No.2) [Knowledge]

2.. Discuss importance of signal gating in low power VLSI design. [5M] (C.O.No.3) [Knowledge]

3. Gate level simulation is an important aspect of VLSI design flow. Illustrate GLS. [5M] (C.O.No.3) [Knowledge]

4 The MTCMOS is one of the low power techniques. Discuss in detail about the MTCMOS. [5M] (C.O.No.3) [Knowledge]

5.. Scaling of a transistor means reducing the critical parameter of the device. List out the advantages of scaling? [5M] (C.O.No.3) [Knowledge]

Part B [Thought Provoking Questions]

Answer any 4 Questions. Each question carries 10 marks. (4Qx10M=40M)

6 Explain about switching power dissipation and short circuit power dissipation. [10M](C.O.No.3) [Comprehension]

7. With usual notations show that dynamic power dissipation in an inverter is given by $P_d=C_LV^2f$. . [10M](C.O.No.2) [Comprehension]

8 Explain the interconnect and layout design techniques for low power design.
[10M](C.O.No.1) [Comprehension]

9 Draw and Explain the flow chart of Monte Carlo based technique for estimation of average power in sequential circuits. [10M](C.O.No.2) [Comprehension]

10. A 32 bit off-chip bus operating at 5V and 66MHz clock rate is driving a capacitance of 25pF/bit. Each bit is estimated to have a toggling probability of 0.25 at each clock cycle. What is the power dissipation in operating the bus? [10M](C.O.No.4) [Comprehension]

11. Compute the transItIon density and static probability of y = ab + c given P(a) = 0.2, P(b) = 0.3, P(c) = 0.4, D(a) = 1, D(b) = 2, D(c) = 3. [10M](C.O.No.4) [Comprehension]

Part C [Problem Solving Questions]

Answer any 3 Questions. Each question carries 15 marks. (3Qx15M=45M)

12. Realize the Boolean function f = $\overline{((A + D\_E) + (B + C))}$. Find an equivalent CMOS inverter circuit for simultaneous switching of all input. Given (W/L)P=15 and for all PMOS and (W/L)N=10 for all NMOS .
15M] (C.O.No.2) [Comprehension]

13. Expalin briefly the following (i) latches (ii) Flip-Flops (iii) Gate Reorganisation . .
[15M] C.O.No.4) [Comprehension]

14 Obtain an expression for capacitive power, internal power and static power dissipation using gate level analysis techniques. [15M](C.O.No.3)[Comprehension]

15. For a Boolean function, F= $\bar{A}\,\bar{B}C + AB\bar{C} + A\bar{B}\bar{C} + \bar{A}\,\bar{B}\bar{C} + ABC + \bar{A}\,B\bar{C}$, draw the BDD and ROBDD diagram. [15M](C.O.No.2) [Comprehension]

16. Determine the switching probability and activity factor for the circuit shown in figure
[15M](C.O.No.4) [Comprehension]