Roll No												

PRESIDENCY UNIVERSITY
BENGALURU

SCHOOL OF ENGINEERING

END TERM EXAMINATION August-2024

Even Semester: M.Tech 2023 - 24
Course Code: ECE5006
Course Name: Hardware Software Co-design
Program & Sem: M.Tech ESV

Date: 13 /08 /2024
Time: 09:30 AM to 12:30 PM
Max Marks: 100
Weightage: 50%

Instructions:
(i) Read the all questions carefully and answer accordingly. All parts are compulsory.
(ii) Do not write any information on the question paper other than Roll Number.

Part A [Memory Recall Questions]

Answer any 3 Questions. Each question carries 5 marks. (3Qx 5M= 15M)

1. A Kahn Process network (KPN) consist of monotonic processes. Describe how KPN is determinate. (CO 1) [Knowledge]

2. System synthesis includes allocation, binding and scheduling. Explain with diagram the process of system synthesis. (CO 2) [Knowledge]

3. Mapping relates application and architecture specifications. Describe specification graph. (CO 3) [Knowledge]

4. In multi-objective optimization explain the black box optimization. (CO 4) [Knowledge]

5. The decision space using the objective function is denoted by objective space. Explain Pareto optimal set. (CO 4) [Knowledge]

Part B [Thought Provoking Questions]

Answer any 4 Questions. Each question carries 10 marks. (4Qx10M=40M)

6. The Integer Programming (IP) model consist of an objective function C involving linear expressions of integer variables from a set X is given below. Determine the optimal solution for the IP. (CO 2) [Comprehension]

Objective function: $C = 3x1 + 5x2 + 7x3$
Subject to: $x1 + x2 + x3 \geq 2$
$x1, x2, x3 \in \{0, 1\}$

7. The system is represented by structural and behavioral objects. Represent the behavioral properties of the following algorithm in control flow graph (CFG) (CO 2) [Comprehension]

```
        Compare_GT_EQ_LT {
1               read (a, b);
2               done = FALSE;
3               repeat {
4                       if(a>b) {
5                               GT = a;
6                               LT = b;}
7                       elseif (b>a) {
8                               GT = b;
9                               LT = a;}
10                      else {
11                              EQ = a;
12                              done = TRUE;}
13              } until done;
14              write (GT, EQ, LT);
        }
```

8. The state set by traversing the tree is represented using the following equation.

$Q_A = (Q_C \cup Q_D) \times (Q_M \cup ((Q_I \cup Q_K) \times Q_L))$

$Q_A = Q_B \times Q_E$

$Q_B = Q_C \cup Q_D$

$Q_E = Q_F \cup Q_M$

$Q_F = Q_G \times Q_H$

$Q_G = Q_I \cup Q_K$

$Q_H = Q_L$

Draw the tree representation for the state set. (CO 1) [Comprehension]

9. Mapping often require only the process network structure and its abstract properties. Derive the equation from the abstraction in data flow graph (DFG) shown in Fig 1.

(CO 3) [Comprehension]

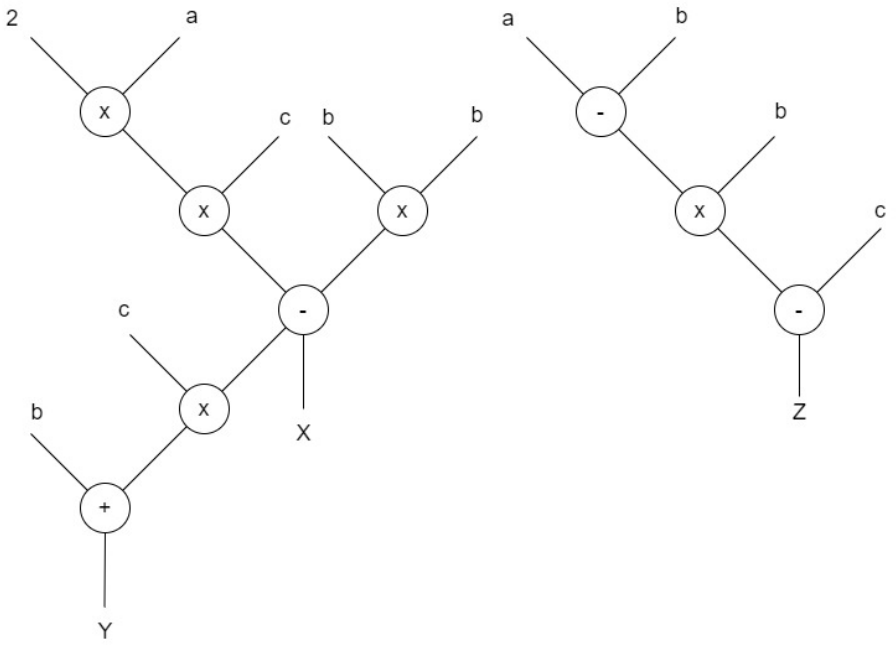

Fig 1

10. A simple producer-consumer application is illustrated in Fig 2. Write program module of simple FIFO read and write interfaces, and FIFO implementation (CO 4) [Comprehension]

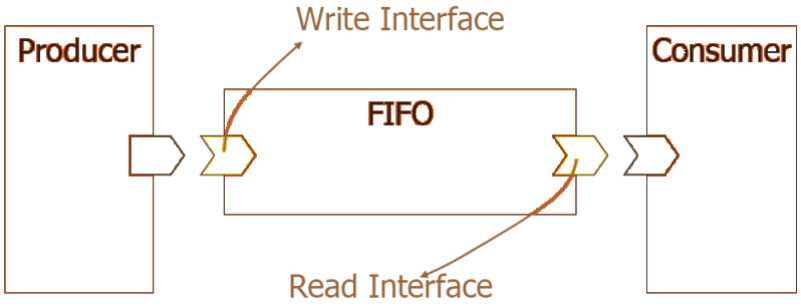

Fig 2

11. The optimization analysis cycle consist of a decision vector X and objective vector f(X). Explain with diagram the optimization analysis cycle. (CO 4) [Comprehension]

Part C [Problem Solving Questions]

Answer any 3 Questions. Each question carries 15 marks. (3Qx15M=45M)

12. A system modeled by an SDF graph has four processes named 'A', 'B', 'C', and 'D', and has the following topology matrix: (CO 1) [Apply]

$$\begin{bmatrix} 4 & -3 & 0 & 0 \\ -2 & 0 & 3 & 0 \\ 0 & 1 & -2 & 0 \\ 1 & 0 & 0 & -3 \\ 0 & 0 & -1 & 2 \end{bmatrix}$$

a. Draw the SDF graph and attach labels to the heads and tails of edges that represent the number of tokens consumed and produced at each firing of the corresponding process.
b. Determine the relative execution rates and periodic schedule.

13. Consider the state chart shown in Fig 3. (CO 2) [Apply]

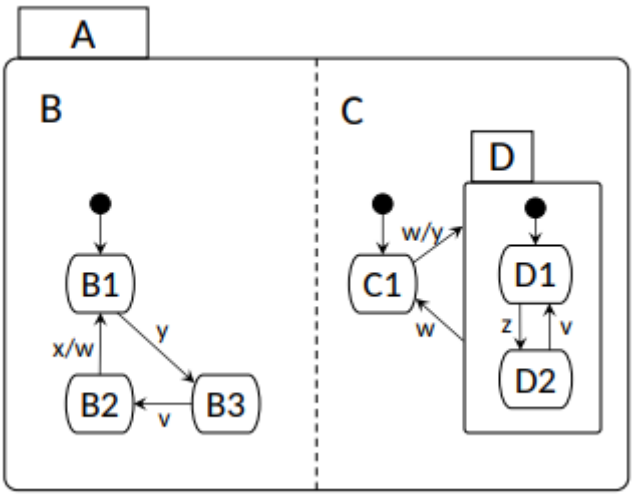

Fig 3

a. Consider the following sequence of external events: x, w, y, y, z, v, x. Determine the sequence of states, the automaton in Fig. passes through, starting from the initial state.
b. Draw a finite state machine (FSM) which is equivalent to the StateChart.

14. Consider the digital circuit shown in Fig 4 (CO 3) [Apply]

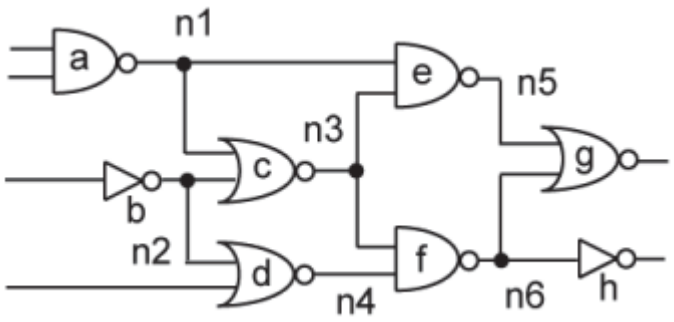

Fig 4

a. Tabulate the cost matrix c(x,y) that assess the communication cost from node x to y.
b. Partition the circuit using the KL algorithm and find the best solution.

15. A comparator is to be designed to compare greater than, equal and less than. Implement in Verilog/VHDL code a 2-bit comparator shown in Fig 5. with Test bench to verify the design. The entity has two 2-bit inputs and three 1-bit outputs. (CO 4) [Apply]

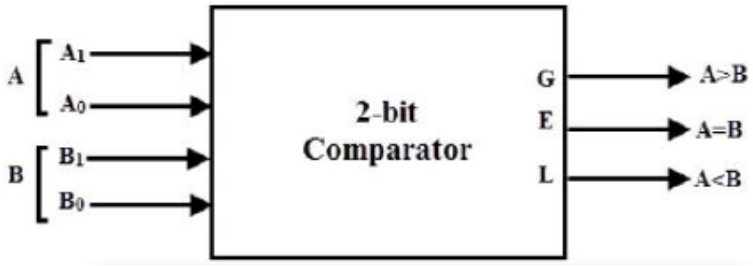

Fig 5

16. Implement in Verilog/VHDL code a 4:1 MUX shown in Fig 6. with Test bench to verify the design. The entity has four 1-bit inputs and one 2-bit select input. The output is a 1-bit wire.
(CO 4) [Apply]

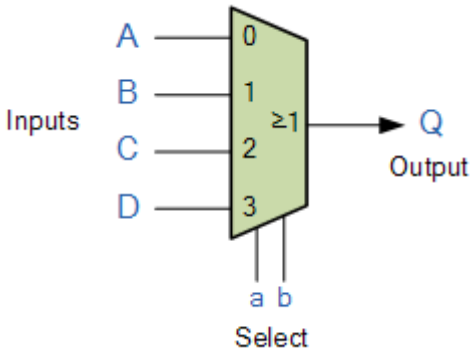

Fig. 6