|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Roll No |  |  |  |  |  |  |  |  |  |  |  |

PRESIDENCY UNIVERSITY BENGALURU

SCHOOL OF ENGINEERING

SUMMER TERM ENDTERM EXAMINATION - AUGUST 2024

|  |  |
| --- | --- |
| **Semester : Summer** | **Date : 07-AUGUST-2024** |
| **Course Code : ECE3001** | **Time : 09:30 AM to 12:30 PM** |
| **Course Name : Linear Integrated Circuits** | **Max Marks : 100** |
| **Program : B.Tech.** | **Weightage : 50%** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

|  |  |  |  |
| --- | --- | --- | --- |
| **PART A** | | | |
| **ANSWER ANY 5 QUESTIONS 5Q X 4M=20M** | | | |
| 1 | An operational amplifier is a multistage, direct coupled, high gain amplifier with two inputs and one output. Sketch the pin diagram of a operational amplifier. | (CO 1) | **[Comprehension]** |
|  | | | |
| 2 | Parameters of an op-amp give an idea about the op-amp when it is used in any electronic circuit. Define SVRR and state the value of this parameter for 741C op-amp. | (CO 1) | **[Comprehension]** |
|  | | | |
| 3 | Parameters of an op-amp give an idea about the op-amp when it is used in any electronic circuit. Define voltage gain or large signal voltage gain and state the value of this parameter for 741C op-amp. | (CO 1) | **[Comprehension]** |
|  | | | |
| 4 | The differential gain of an op-amp is and the common mode gain is 0.001. Find the CMRR in linear scale and in dB. | (CO 1) | **[Comprehension]** |
|  | | | |
| 5 | An amplifier using an op-amp with a slew rate of 𝟏𝑽/𝝁𝒔 has a gain of 40 dB. If this amplifier is to faithfully amplify sinusoidal signals from dc to 20 KHz, without any slew rate induced distortion, what is the maximum input that can be applied? | (CO 1) | **[Comprehension]** |
|  | | | |
| 6 | An op-amp with slew rate of 𝟖 𝑽/𝝁𝒔 is driven by a 250 kHz sine wave. What is the maximum output voltage at which slew rate limit is reached? | (CO 1) | **[Comprehension]** |
|  |  |  |  |
|  | | | |

|  |  |  |  |
| --- | --- | --- | --- |
| **PART B** | | | |
| **ANSWER ANY 4 QUESTIONS 4Q X 10M=40M** | | | |
| 7 | An inverting amplifier is an amplifier using operational amplifier which provides a negative gain to the input signal applied. Design an inverting amplifier for a gain of -10 | (CO 2) | **[Application]** |
|  | | | |
| 8 | A subtractor or a difference amplifier is an electronic circuit which will subtract one signal from another signal. Draw the circuit diagram of a subtractor and derive the expression for its output voltage. | (CO 2) | **[Application]** |
|  | | | |
| 9 | A Schmitt trigger or a squaring circuit uses positive feedback. Draw the circuit diagram, input waveform, output waveform, and the transfer characteristics of an inverting Schmitt trigger. Also, derive the expression for the hysteresis voltage. | (CO 3) | **[Application]** |
|  | | | |
| 10 | Design a non-inverting Schmitt trigger for a lower threshold point of -5V and an upper threshold point of 5V. Draw the input waveform, output waveform and the transfer characteristics if the input is a 20V peak to peak sine wave. Given | (CO 3) | **[Application]** |
|  | | | |
| 11 | A successive-approximation register ADC is a type of analog-to-digital converter that converts an analog voltage into its equivalent digital representation using a binary search through all possible quantization levels before finally converging upon a digital output for each conversion. Draw the block diagram of a successive-approximation register type ADC and explain its operation by considering the digital equivalent of the analog input data to be converted to be 1010. | (CO 3) | **[Application]** |
|  | | | |

|  |  |  |  |
| --- | --- | --- | --- |
| **PART C** | | | |
| **ANSWER ANY 2 QUESTIONS 2Q X 20M=40M** | | | |
| 12 | The R 2R Ladder DAC requires only resistors with values R and 2R. Draw the circuit diagram of a 2-bit R 2R DAC. Find the expression for the output voltage in each case and the general expression. Let find the output voltage in each case. | (CO 4) | **[Application]** |
|  | | | |
| 13 | A 2-bit binary weighted resistor DAC will have the resistors 𝑅, 2𝑅. A 3-bit binary weighted resistor DAC will have the resistors 𝑅, 2𝑅, 4𝑅. Draw the circuit diagram of a 2-bit binary weighted resistor DAC. Find the expression for the output voltage in each case and the general expression. Let find the output voltage in each case. | (CO 4) | **[Application]** |
| 14 | An n-bit flash ADC requires resistors and comparators. Draw the circuit diagram of a 2-bit flash ADC. Analyze all the four cases. Also, design the 3:2 Encoder present in a 2-bit flash ADC. | (CO 4) | **[Application]** |
|  | | | |