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PRESIDENCY UNIVERSITY BENGALURU

 SCHOOL OF ENGINEERING

 END TERM EXAMINATION (SUMMER TERM) – AUGUST 2024

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| **Semester : V** | **Date : 6.8.2024** |
| **Course Code :ECE3008** | **Time : 1.00pm to 04.00pm** |
| **Course Name :VLSI Design** | **Max Marks :100** |
| **Program :B.Tech (ECE)** | **Weightage :50%** |

**Instructions:**

1. *Read all questions carefully and answer accordingly.*
2. *Question paper consists of 3 parts.*
3. *Scientific and non-programmable calculator are permitted.*
4. *Do not write any information on the question paper other than Roll Number.*

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| **PART A** |
|  **ANSWER ANY 5 QUESTIONS 5Q X 4M=20M** |
| 1 | Illustrate RTL and Place and route in Verilog HDL. | (CO 1) | [Knowledge] |
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| 2 | List and explain two fabrication steps in VLSI based transistors. | (CO 1) | [Knowledge] |
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| 3 | Write a Verilog HDL code for two input AND gate using behavioral and gate level modelling. | (CO 2) | [Knowledge] |
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| 4 | What is electron affinity and work unction? | (CO 2) | [Knowledge] |
| 5 | Illustrate Twin tub process. | (CO 2,) | [Knowledge] |
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| 6 | List out the different parameters in threshold volage. | (CO 2) | [Knowledge] |
| 7 | Current in the MOSFET is a function of gate-to-source voltage and drain-to-source voltage. What are the current equations for MOSFET? | (CO 2) | [Knowledge] |
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| **PART B** |
|  **ANSWER ANY 4 QUESTIONS 4Q X 10M=40M** |
| 8 | Flip flop is one bit storage element. Write a Verilog for D and SR FF.  | (CO 3) | [Comprehension] |
| 9 | A full adder is a basic building block in parallel adder circuit. Write a Verilog HDL code for full adder using data flow and gate level modelling. |  |  |
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| 10 | CMOS is the semiconductor technology used in most of today's digital circuits. Realize the Boolean function$ F=\overline{A+\overline{(\overline{B}+CD)}}$ using CMOS technology. | (CO 3) | [Comprehension] |
| 11 | Stick diagrams shows the layers used and the relative position of the layerDesign two input NOR gate using CMOS Technology and draw the stick diagram with Euler’ graph. | (CO 4) | [Comprehension] |
| 12 | CMOS inverter includes one PMOS and one NMOS transistor. (i) What is the switching threshold in a CMOS inverter? (ii) Describe noise margin. | (CO 4) | [Comprehension] |
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| 13 | Transistors are used as electronics switches. Draw the input and output characteristics of an MOSFET and mark the region of operation. | (CO 4) | [Comprehension] |
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| **PART C** |
|  **ANSWER ANY 2 QUESTION 2Q X 20M=40M** |
| 14 | (a) Digital inverter quality is often measured using the Voltage Transfer Curve (VTC), which is a plot of input vs. output voltage. Explain in detail about VTC of CMOS inverter. (10)(b) Stick diagrams are a means of capturing topography and layer information using simple diagrams. Design two input NAND gate using CMOS Technology and draw the stick diagram with Euler’ graph. (5)(c) Design rules represent a tolerance which insures very high probability of correct fabrication. Illustrate Well rules in Layout design. (5) | (CO4, 5) | [Application] |
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| 15 | (a) PTL (Pass Transistor Logic) is an area efficient technology in VLSI. Implement two input AND, OR, NAND, NOR and EX-OR gates using PTL and design 4:1 mux using Transmission gates. (15)(b) Dynamic Random Access Memory (DARM) uses only one transistor to store one bit of information. Explain in detail about DRAM-1T with neat diagram. (5) | (CO 5) | [Application] |
| 16 | (a) The reduction of all dimensions of the chip by a factor of “s” is called scaling. Scale the below parameters using the three scaling techniques. (i) Gate Area (ii). Gate capacitance per unit area  (iii). Charge density in the channel (iv). Channel resistance. (10)(b) MOS transistors suffer from unwanted parasitic effects. One such problem in MOSFET is latch up. With a neat figure explain latch up and mention its prevention techniques. (10)  | (CO4, 5) |  |
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